Solid-State Electronics 125 (2016) 82–102

Contents lists available at ScienceDirect

Solid-State Electronics

journal homepage: www.elsevier.com/locate/sse

III-V/Ge MOS device technologies for low power integrated systems

S. Takagi [a,b,*], M. Noguchi [a], M. Kim [a,b], S.-H. Kim [a,b,c], C.-Y. Chang [a,b], M. Yokoyama [a,b], K. Nishi [a,b], R. Zhang [a,d], M. Ke [a,b], M. Takenaka [a,b]

[a] Department of Electrical Engineering and Information Systems, The University of Tokyo, 7-3-1 Hongo, Bunkyo-ku, Tokyo 113-8656, Japan
[b] JST-CREST, 7-3-1 Hongo, Bunkyo-ku, Tokyo 113-8656, Japan
[c] Korea Institute of Science and Technology, Seoul 136-791, Republic of Korea
[d] Zhejiang University, Hangzhou 310027, China

ARTICLE INFO

Article history:
Available online 20 July 2016

The review of this paper was arranged by Jurriaan Schmitz

Keywords:
MOSFET
Tunneling FET
Germanium
III-V semiconductors
Metal-Oxide-Semiconductor
Mobility
Interface states

ABSTRACT

CMOS utilizing high mobility III-V/Ge channels on Si substrates is expected to be one of the promising devices for high performance and low power integrated systems in the future technology nodes, because of the enhanced carrier transport properties. In addition, Tunneling-FETs (TFETs) using Ge/III-V materials are regarded as one of the most important steep slope devices for the ultra-low power applications. In this paper, we address the device and process technologies of Ge/III-V MOSFETs and TFETs on the Si CMOS platform. The channel formation, source/drain (S/D) formation and gate stack engineering are introduced for satisfying the device requirements. The plasma post oxidation to form GeO_x interfacial layers is a key gate stack technology for Ge CMOS. Also, direct wafer bonding of ultrathin body quantum well III-V-OI channels, combined with Tri-gate structures, realizes high performance III-V n-MOSFETs on Si. We also demonstrate planar-type InGaAs and Ge/strained SOI TFETs. The defect-less p^+-n source junction formation with steep impurity profiles is a key for high performance TFET operation.

1. Introduction

Low power consumption is of paramount importance for advanced CMOS (Complementary Metal-Oxide-Semiconductor)-based logic LSI (Large-Scale Integrated circuits) and integrated systems mainly because of the difficulty in supply voltage (V_{dd}) reduction under realistic CMOS device design. Actually, the V_{dd} lowering is the most effective way in reducing the power consumption of CMOS, P_{consum}, seen in (1).

$$P_{consum} \approx afC_{load}V_{dd}^2 + I_o \cdot 10^{-V_{th}/S} \cdot V_{dd} + I_{leak} \cdot V_{dd} \quad (1)$$

where a, f, C_{load}, I_0, S and I_{leak} are a constant value, the operating frequency, the load capacitance, the drain current at $V_g = V_{th}$, the sub-threshold slope and the additional leakage currents including gate and junction leakages, respectively [1]. Here, the first term corresponds to the dynamic power, while the second and third terms correspond to the static power. In both components, the lowering of V_{dd} can effectively reduce the power consumption.

While the steady progress in suppression of short channel effects and reduction in equivalent oxide thickness can contribute to lowering V_{dd} to some extent, the significant reduction in V_{dd} is difficult for Si CMOS. Here, there are two possible strategies to further reduce V_{dd}. These strategies are schematically shown in Fig. 1. One way is to employ channel materials with higher source injection velocity such as Ge and III-V compound semiconductors. Under ballistic transport limit, on-current, I_{on}, can be simply represented [2–5] by

$$I_{on} = qN_s v_{inj} \approx C_g(V_{dd} - V_{th})v_{inj} \quad (2)$$

where q, N_s, v_{inj}, C_g and V_{th} are elemental charge, surface carrier concentration at source edge, carrier injection velocity at source edge, gate capacitance and threshold voltage, respectively. Since semiconductor channel materials with lower effective mass such as Ge and III-Vs are known to lead to higher injection velocity, higher I_{on} can be obtained at a given value of V_{dd} [6,7]. As a result, the III-V/Ge MOSFETs can reduce N_s under a given I_{on} value, resulting in the reduction in V_{dd}, as shown in (2) and Fig. 1. This strategy can contribute to reduction of gate overdrive.

The typical CMOS structures composed of III-V/Ge channels are schematically shown in Fig. 2 [8–10]. Here, Ge with the significantly light hole and light electron effective mass is suitable for p-channel MOSFETs or CMOS applications. In particular, Ge CMOS is plausible in terms of the simplicity of the process/material integration, because the CMOS is composed of a single material. Also,

* Corresponding author at: Department of Electrical Engineering and Information Systems, The University of Tokyo, 7-3-1 Hongo, Bunkyo-ku, Tokyo 113-8656, Japan.
E-mail address: takagi@ee.t.u-tokyo.ac.jp (S. Takagi).

http://dx.doi.org/10.1016/j.sse.2016.07.002
0038-1101/

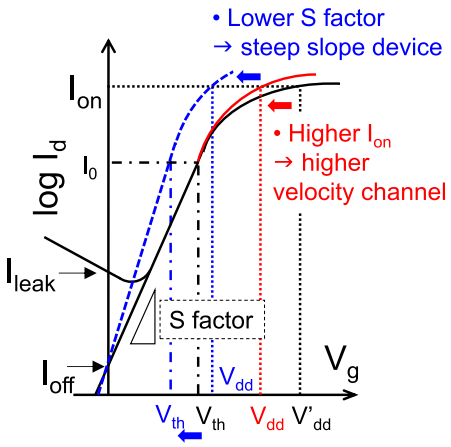

Fig. 1. Two possible strategies to further reduce V_{dd}.

In-based III-V semiconductors such as InGaAs, InAs and InSb with the quite light electron effective mass are suitable for n-channel MOSFET applications, while Sb-based III-V semiconductors such as GaSb, InGaSb and InSb with the light hole effective mass are suitable for p-channel MOSFETs or CMOS applications. Although III-V CMOS is another possible CMOS structure, there can still be many choices of materials for CMOS. This is because III-V materials suitable for n-MOSFETs and p-MOSFETs are different in most cases. Among them, one of the ultimate CMOS structures can be the co-integration of an In-based III-V n-MOSFET and a Ge p-MOSFET [8,9], because of the superior physical properties including the carrier transport ones as well as the contact resistance with metals.

On the other hand, the other strategy for the reduction in V_{dd} is to introduce devices with steep slope of the channel current change in sub-threshold region. This way can contribute to the reduction in V_{dd} by decreasing the gate voltage swing in the sub-threshold region, as also shown in Fig. 1. Here, the inverse of the slope of the channel current change with respect to gate voltage, V_g, defined as the sub-threshold slope (S.S.), which is the V_g change necessary to change channel currents by one order of the magnitude, is known to have the minimum value of ~60 mV/dec at room temperature for conventional MOSFETs dominated by thermionic current in sub-threshold region. Thus, any new device operation mechanisms are needed to realize sub-threshold slope lower than this minimum value.

One of the most promising steep slope devices can be tunneling FETs (TFETs) [11–14], where tunneling probability and resulting tunneling current are modulated by V_g. Typical TFET structures are also shown in Fig. 2. This is because a variety of simulation results have reported the excellent performance of TFETs with the steep slopes [11,13] and, actually, the device operations with sub-threshold slope less than 60 mV/dec in a low V_{dd} region typically less than 0.5 V, have already been demonstrated without large hysteresis [15–22]. Also, fabrication of some of TFETs can be regarded as highly compatible with the Si CMOS platform. However, one of the drawbacks in TFETs is the low current drive [11–14], attributed to low tunneling probability. Particularly, Si-based TFETs are known to have the essential limitation in I_{on} and S.S. [11–14], because of the high bandgap energy, E_g, and the indirect bandgap. Thus, III-V/Ge is promising for the materials used in TFETs as well, because of lower E_g, direct bandgap in III-V and various possible combinations of the hetero-structures, which lead to the higher tunneling probability. Here, it is known that the source/channel junctions composed of type-II hetero-structures are effective in enhancing I_{on} of TFETs with maintaining low off current. It has been recognized from this viewpoint that $In_xGa_{1-x}As/GaAs_y$-Sb_{1-y} and Si/Ge hetero-interfaces are suitable for advanced TFETs.

As a result, the heterogeneous integration of III-V/Ge with the Si CMOS platform is a promising direction for realizing ultra-low power CMOS and TFETs along More Moore and Beyond CMOS approaches, respectively, in the 10 nm technology nodes and beyond, where ultra-low power integrated systems are indispensable. In addition, a combination of III-V/Ge-based photonic devices with advanced CMOS can also provide another possible system solution through optical interconnect for minimizing the power consumption of the interconnect under a given system performance, though this aspect is not touched on in this paper.

On the other hand, there are still many critical issues and difficult challenges for realizing III-V/Ge-based CMOS and TFETs on the Si platform [8–10,14], which are schematically shown in Fig. 3. These include (1) formation of high-crystal-quality Ge/III-V films on Si substrates, where ultrathin body III-V-OI/GOI structures are needed with combination of any carrier transport booster technologies, (2) gate stack technologies to realize superior MOS interface quality, leading to MOS gate stacks with ultrathin equivalent oxide thickness (EOT) and low densities of interface states and border traps, high channel mobility and high gate stack reliability including long term threshold voltage (V_{th}) stability, (3) the formation of source/drain (S/D) with low resistivity and low leakage

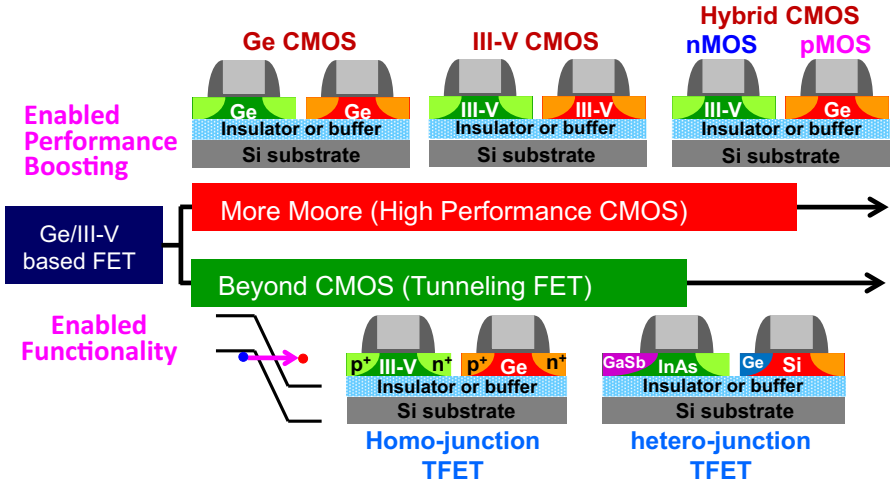

Fig. 2. Possible structures for advanced MOSFETs and TFETs using III-V/Ge devices on Si platform through heterogeneous integration.