Solid-State Electronics xxx (2016) xxx–xxx

Contents lists available at ScienceDirect

Solid-State Electronics

journal homepage: www.elsevier.com/locate/sse

Post drain-stress behavior of AlGaN/GaN-on-Si MIS-HEMTs

Simon A. Jauss [a,*], Stefan Kilian [a], Stephan Schwaiger [a], Stefan Noll [a], Walter Daves [a], Oliver Ambacher [b]

[a] Robert Bosch GmbH, Robert-Bosch-Campus 1, 71272 Renningen, Germany
[b] Fraunhofer Institute for Applied Solid State Physics, Tullastraße 72, 79108 Freiburg, Germany

ARTICLE INFO

Article history:
Available online xxxx

The review of this paper was arranged by Jurriaan Schmitz

Keywords:
GaN
HEMT
Trapping
Stress

ABSTRACT

In this paper we investigate the drain stress behavior and charge trapping phenomena of GaN-based high electron mobility transistors (HEMTs). We fabricated GaN-on-Si MIS-HEMTs with different dielectric stacks in the gate and gate-drain access region and performed interface characterization and stress measurements for slow traps analysis. 2-dimensional TCAD simulations were used to compare the electrical field distributions of the devices in OFF-state stress condition. Our results show a high dependency of the on-resistance increase on interfaces in the gate-drain access region. The dielectric interfaces near the channel play a significant role for long term high voltage stress and regeneration of the device.

1. Introduction

GaN-based high electron mobility transistors (HEMTs) are promising candidates for future power electronics applications because of high electrical breakdown fields (3.9 MV/cm) and a 2-dimensional electron gas (2DEG) induced high electron mobility [1,2]. Major issues to be solved are long term reliability and charge trapping phenomena that limit the dynamic performance of the devices. The so-called 'current collapse', i.e. the decrease in drain current in dynamic operation, in particular is under strong investigation, also for MIS (Metal-Isolator-Semiconductor)-HEMTs [3]. This effect is related to deep levels charge trapping, induced by electrical stress [4], leading to channel depletion and a voltage shift.

Different regions have been localized where trapping effects, and thus current collapse, occurs [5,6]. The first region is at the gate edge to the drain side due to an electric field peak while stressing the device with high drain voltage in the OFF-state. This effect can be reduced by optimizing the device geometry (e.g. by an appropriate design of field plates at source and gate) [7,8]. The second region is the buffer where traps limit the dynamic device performance [9]. The third region is the gate-drain access region, which is decisive for the dynamic behavior [10]. It has been shown that a passivation layer (e.g. silicon nitride) can saturate surface traps on the semiconductor to prevent charging effects [11].

In this paper, we compare MIS devices with different passivation layers in the access region by CV-measurements for interface characterization, as well as stress measurements for device performance comparison, including results published in [12]. By TCAD simulations, the electrical field distributions of the devices are compared and the results are verified. We demonstrate a large influence of the thickness and deposition method of the first passivation layers in the access region on charge trapping and device behavior under stress.

2. Device fabrication

We fabricated AlGaN/GaN MIS-HEMTs and test structures on MOCVD grown GaN-on-Si wafers with a 2.4 µm GaN buffer and a 25 nm $Al_xGa_{1-x}N$ barrier with $x = 0.25$. Device I, shown in Fig. 1 (a), was passivated by a 10 nm MOCVD SiN layer, which was used as the gate dielectric. Ohmic contacts have been created by sputter deposition and lift-off of Ti/Ni/Al/Au, followed by an annealing step at 850 °C for 30 s. Subsequently, Al metal was deposited followed by a 300 nm SiN passivation by inductive coupled plasma chemical vapor deposition (ICPCVD) at 300 °C and the Al power metallization including source field plates. In device II (Fig. 1(b)), a second gate dielectric (CVD SiO_2) was deposited on top of the MOCVD SiN after surface cleaning. For devices III and IV the MOCVD in situ SiN was replaced by a 2 nm GaN cap and a 12 nm LPCVD SiN layer was deposited to work as gate dielectric. An alternative design was obtained for device IV by the deposition of 100 nm LPCVD SiN as passivation in the access region. The gate foot was opened by a soft dry etch process. After surface treatment the

* Corresponding author.
E-mail address: SimonAlexander.Jauss@de.bosch.com (S.A. Jauss).

http://dx.doi.org/10.1016/j.sse.2016.07.014
0038-1101/

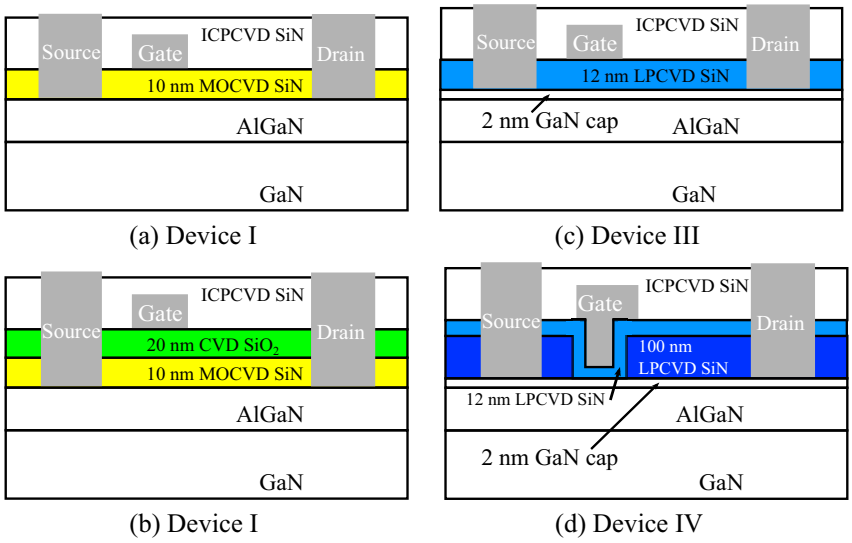

Fig. 1. Device structure of processed transistors with the following dielectric layers in the gate drain access region: (a) MOCVD SiN, (b) MOCVD SiN/CVD SiO_2, (c) LPCVD SiN, (d) Alternative design with 100 nm thick LPCVD SiN, gate field plate and 12 nm LPCVD SiN as gate dielectric.

SiN gate dielectric was deposited. The four different access regions in the devices I–IV are shown in Fig. 1:

- Device I: MOCVD SiN (in situ)/ICPCVD SiN
- Device II: MOCVD SiN (in situ)/CVD SiO_2/ICPCVD SiN
- Device III: LPCVD SiN/ICPCVD SiN
- Device IV: LPCVD SiN

3. Measurement setup

For the characterization we used transistors with a gate length of 2 µm and a gate width of $W_G = 50$ µm, as well as capacitance structures of 0.09 mm² and 0.01 mm². The transfer characteristics and gate leakage current of devices I–IV are shown in Fig. 2(a). The gate current was very low within a wide bias range in all devices. The threshold voltage varies between $V_{th} = -4$ V and $V_{th} = -9$ V due to different equivalent oxide thicknesses (EOT) of the devices. The On/Off-current ratio is around 10^9, whereas both the drain current I_D and the gate current I_G are the lowest for LPCVD SiN as the first passivation layer in device III. Device IV with the same gate dielectric as device III exhibited a comparable output characteristic as shown in Fig. 3. The electrical breakdown was measured at $V_D = 400$ V–500 V using a current criteria of $I_{D,BD} = 10^{-4}$ A/mm.

For gate dielectric characterization, frequency-dependent capacitance-voltage (CV) measurements have been used, using the Agilent E4989A LCR-Meter. In Fig. 2(b), the CV-characteristics of all devices are plotted. They show a hysteresis-free behavior when biasing to the low positive voltage range, indicating a good interface. To determine the interface trap density of the different interfaces GaN-AlGaN and SiN-AlGaN, we used the conduction method described in [13]. We extracted similar trap densities between $D_{it} = 4 \times 10^{11}$ cm^{-2} and $D_{it} = 5.5 \times 10^{11}$ cm^{-2} in the different devices shown in Table 1 for the heterointerface GaN/AlGaN. For the interface between the AlGaN/GaN cap and the dielectric layer, we determined trap densities of $D_{it} = 3 \times 10^{11}$ cm^{-2}–8.7×10^{11} cm^{-2}, also listed in Table 1. Deep traps cannot be measured using this technique, so that the trap density could be higher, especially for the AlGaN/SiN interface. Transistors in power applications need to withstand high blocking voltages up to $V_D = 600$ V and are biased within a gate voltage swing of $\Delta V_G = 20$ V, e.g. from $V_G = -15$ V to $V_G = 5$ V. For the evaluation of the stress behavior, a measurement routine as in Fig. 4 has been developed using the Keithley 2636A and 2657A sourcemeters. First, an I_D/V_G transfer characteristic at $V_D = 1$ V has been measured. This is indicated in Fig. 4 by the black arrow. Second, the transistors were stressed for 10 s with a drain[1] voltage $V_D = 20$ V, followed by another measurement of the transfer characteristic (red arrow). Third, this was repeated with $V_D = 100$ V during the stress period followed by a final transfer characteristic I_D/V_G. These I_D/V_G-measurements were done <5 ms after stress, therefore shallow traps with time constants of $\tau < 10^{-3}$ s are not visible.

4. Result and discussion

Fig. 5 shows the result of devices I–IV. All of them have a gate-drain distance of $L_{GD} = 16$ µm and possess a source field plate of $L_{SFP} = 4$ µm from the gate edge to the drain side. The gate and drain leakage currents of all devices also stayed low under stress. Device I in Fig. 5(a) shows a large increase of $R_{DS,on}$, where $r_{DS} = R_{DS,post\ stress}/R_{DS,initial} = 1.22$, after $V_G = 20$ V stress and $r_{DS} = 2.6$ after $V_D = 100$ V stress. The shape of the I_D/V_G-characteristics without a shift of V_{th} and an increase of R_{on} indicates trap charging in the gate-drain access region [5]. Fig. 5(c) displays that LPCVD SiN as a gate dielectric (device III) leads to a considerably smaller increase of on-resistance. A change in the current degradation behavior of the devices could not be seen when changing the OFF-state gate voltage to consider the different EOTs and related different gate stress conditions. Only a slight change of the threshold voltage (<0.5 V) could be seen, which was not related to with drain-based stress. A dominant trapping in the gate-drain access region can also be seen in device II. R_{on} increases to $r_{DS} = 1.02$ and $r_{DS} = 1.06$ for $V_D = 20$ V and $V_D = 100$ V, respectively. This is surprising, since the semiconductor-SiN interface of device I is considered to be excellent [14,15]. Since the interface characterization of the AlGaN/GaN and the AlGaN/SiN interfaces does not show significantly different trap densities, we attribute this effect to the SiN-SiN interface at the drain-gate access region, as is demonstrated in Fig. 6(a). The better performance of device III compared to device I could be due to charges in the GaN cap inter-

[1] For interpretation of color in 'Fig. 4', the reader is referred to the web version of this article.

Please cite this article in press as: Jauss SA et al. Post drain-stress behavior of AlGaN/GaN-on-Si MIS-HEMTs. Solid State Electron (2016), http://dx.doi.org/10.1016/j.sse.2016.07.014