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Impact of temperature and programming method on the data retention of Cu/Al_2O_3-based conductive-bridge RAM operated at low-current (10 μA)

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ABSTRACT

In this paper we outline the effects on the memory window of the programming method and pulse width and of the temperature, in Cu/Al_2O_3-based CBRAM targeting a 10-μA current regime. Despite its large median value, the overall HRS/LRS ratio in these devices can be drastically reduced due to the LRS and HRS dispersion and to the instability of the resistive states over time, especially in a low-current regime. For this reason, in this study we adopt a statistical approach, focusing on the tails of the cumulative distribution Function (CDF). We compare different verify-based algorithms to force an initial tail-to-tail (1st percentile of CDF) resistive window, demonstrating that, in order to reduce the total programming time, a complete Write/Erase cycle must be performed at each verify attempt. We also prove that the stability of the programmed LRS/HRS states is strongly influenced by the external temperature and that it is affected by the programming pulse width (PW) used in the algorithm, likely driving the diffusion processes that originate the state degradation. Selecting the appropriate PW, no overlap of the LRS and HRS distributions is observed after 1 week at room temperature.

1. Introduction

Within the broad spectrum of emerging memory devices, Resistive Random Access Memory (RRAM), where the memory operation relies on the switching of the device resistance, are attracting an ever increasing interest, mainly due to their ease of integration [1]. A specific RRAM concept, Conductive-Bridge Random Access Memory (CBRAM), is based on the voltage-driven commutation of the resistance between a high-resistive state (HRS) and a low-resistive state (LRS) and vice versa, due to the electrochemical formation/dissolution of a metallic filament in a solid electrolyte. Its structure is made by a solid electrolyte thin film sandwiched between an electrochemically active electrode and an inert electrode. During the writing operation (SET), where the metallic filament is created, a positive voltage is applied to the active electrode, whereas the erase operation (RESET) is performed by applying a negative voltage on the same electrode. Among all the types of Resistive Random Access Memory (RRAM), CBRAM is nowadays considered one of the most promising candidates for future non-volatile memory replacement, thanks to its fast low-power operation, long endurance lifetime, good data retention [2–5] and optimal robustness to ionizing radiations [6].

Nevertheless, reliability issues are still hindering the introduction of CBRAM into the memory market. In particular, it has been demonstrated that RRAM devices are subjected to a large increase of the bit dispersion, to a reduction of the overall resistive window, and to a data retention loss when the current is decreased to the sub-10 μA regime [7,8]. As additional reliability concern of CBRAM, resistance drift over time has been reported [9].

We already reported, for Cu/Al_2O_3-based CBRAM devices, fast and low-power switching and large resistive window ($RW = R_{HRS}/R_{LRS}$) for an operating (forming and SET) current $I_{OP} = I_{form} = I_{SET} = 10$ μA [10]. We demonstrated that, when cycle-to-cycle and device-to-device dispersions are taken into account, the overall resistive window is drastically reduced [11]. As reported in [12], the resistive window level can be forced by adopting program/verify algorithms, and we demonstrated that CBRAM devices ensure a shorter programming time with respect to OxRRAM, due to the larger and more controllable initial resistive window. In Ref. [13], we also identified the most efficient algorithm and its impact on the state instability of the devices. In this paper, we provide additional details about the selection of the most efficient algorithm, and we demonstrate that a minimum write time is necessary to have an

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effective verified programming. We also thoroughly analyze the state instability of these devices, and its dependence on the write pulse width and on the initially programmed state. Finally, we demonstrate that the state instability is strongly accelerated by temperature, and, based on the experimental results and on the physical mechanisms previously reported to drive the retention loss, we eventually discuss the origin of the state degradation in these devices.

2. Experimental

The device is integrated on the drain of a select transistor in a 1-Transistor/1-Resistor (1T1R) configuration (Fig. 1a).

The bottom electrode (BE) is a 90-nm wide W-plug. Then a 3-nm thick Al_2O_3 layer is deposited by an H_2O-based Atomic-Layer-Deposition (ALD) technique at 300 °C. The top electrode (TE) consists of a 10 nm-thick TiW (25 at.% Ti) liner preventing Cu in-diffusion [9] and a Cu layer realized in a single-damascene process. Finally, the devices are passivated by Si_3N_4 and SiO_2 [9].

The electrical characterization was carried out by means of an Agilent B1500 semiconductor parameter analyzer for quasi-static (DC) measurements. The pulse-driven (AC) programming was performed by means of a dedicated setup, including a pulse generator for programming the devices and a parameter analyzer for reading the states after each pulse at 0.1 V. The SET and RESET operations are performed by applying a positive (resp. negative) voltage on the bit line (BL). The current level during forming/SET is controlled by applying the proper voltage on the word line (WL). For all the tests reported in this paper the WL voltage is adjusted to obtain a current level of 10 μA.

3. Results

3.1. Single-pulse programming

Fig. 2 reports the DC characteristics and the write endurance statistics of the W/Al_2O_3/TiW/Cu devices. The low pre-forming leakage shown in Fig. 2a indicates that the TiW layer acts as an effective Cu buffer (Fig. 2b), suggesting good potential for deep HRS in the following cycles. After forming, it can be systematically switched with reproducible *I–V* characteristics, exhibiting a resistive window of ~10^4. By writing with short pulses (10 ns), 10^6 cycles can be systematically reached with RW ≈ 100 (Fig. 2c). In Fig. 3 we report typical cycle-to-cycle (C2C) AC-switching statistics of LRS and HRS collected for $PW_{SET,RESET}$ = 100 ns. A resistive window RW ~100 is extracted at 50% of the distribution. However, due to the C2C dispersion of the programmed states, which affects the resistive window more than the device-to-device (D2D)

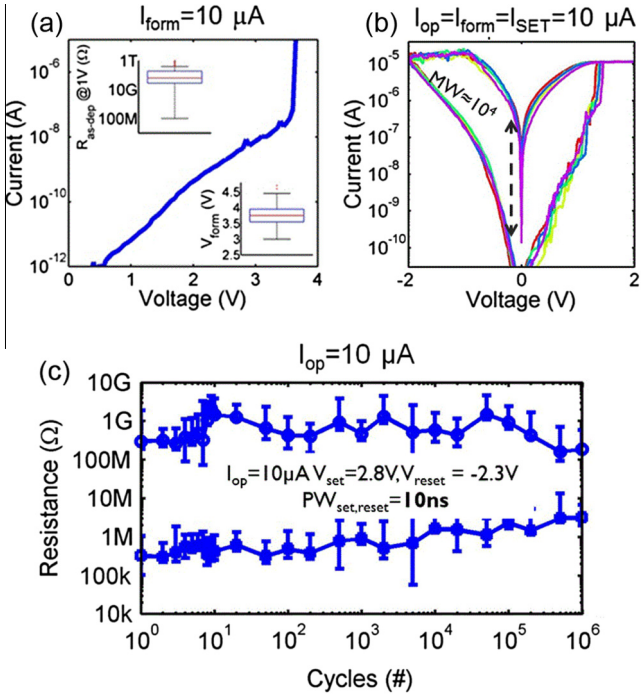

Fig. 2. (a) Typical forming characteristic of the W/Al_2O_3/TiW/Cu devices and data sets of initial resistance and forming voltage V_{form} (insets); (b) DC switching characteristics for I_{OP} = 10 μA, highlighting the large memory window; (c) Write endurance characteristics for 20 devices obtained by applying 10-ns pulses.

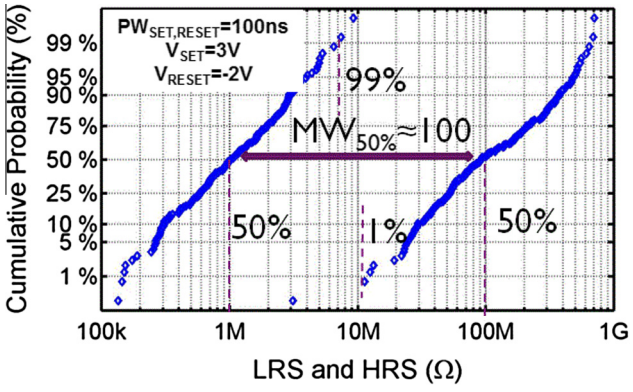

Fig. 3. Cycle-to-cycle (C2C) CDF of LRS and HRS collected for 100 ns-short write pulses, with the inset reporting the switching conditions used for this test.

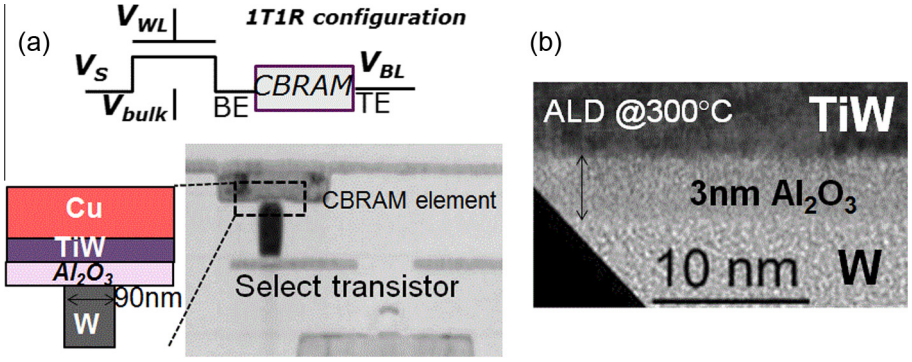

Fig. 1. (a) Schematics and Transmission Electron Microscopy (SEM) image of the 1T1R CBRAM cell stacked on 90 nm W-plug; (b) TEM of the stack under investigation.

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