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Experimental location of damage in microelectronic solder joints after a board level reliability evaluation

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ABSTRACT

Reliability evaluation of integrated circuit (IC) packages to assess drop impact is critical, especially in the case of handheld electronic products. The objective of this study is to experimentally identify the location of damage in solder joints in electronic packaging after a board level reliability (BLR) evaluation. The BLR drop test is a useful way to characterize the drop durability of different soldered assemblies onto a printed circuit board (PCB). It is also of great importance when there is a need to evaluate the solder joint between the chip package and PCB through a daisy-chained structure during the evaluation period. However, there is no detailed information available on a pattern ground with a hatched copper PCB layout for high speed responses that are closely related to actual working conditions. In this paper, a fault location on a daisy-chained structure with a pattern ground is shown through a non-destructive analysis using a time-domain reflectometry (TDR) approach. The results obtained in this project indicate that the TDR approach can be used to detect the location of a crack in the string based on changes in the waveform response. The fault location in critical solder balls as predicted by TDR correlate well with experimental observation by cross-section.

1. Introduction

Recently, handheld electronic products have become personal necessities that are in use daily. These products include smart phones, smart watches, tablet PCs, audio players, games, and even more advanced applications, such as biosensors or wearable devices. Benefits of these devices include a combination of a stacked package and small footprint. As a result, the use of stacked board packaging has become rapid and widespread. From the perspective of product reliability, these devices are likely to be dropped during the product's usable lifetime. Therefore, this kind of portable product must pass a board level reliability (BLR) drop test before hitting the market. Therefore, a BLR evaluation of assemblies subjected to a drop impact is a major concern.

There is a growing interest and need for the assessment of board-assembled stacked package solder joint reliability using a board level drop test. With the decrease in size of handheld electronic products, the frequency of accidental drops has increased. Such drops can cause solder joint microcracks that eventually lead to the failure or malfunctioning of the product. There have been many different types of studies, and some have been conducted to determine the reliability performance of integrated circuit (IC) packages during a drop impact test [1–5]. In this paper, a BLR drop test is intended to evaluate and compare the drop impact performance of surface mount electronic components in an accelerated test environment. The excessive flexure of the printed circuit board (PCB) with IC packages may cause interconnect or product failure. The BLR drop test is a destructive test, and the connection is most

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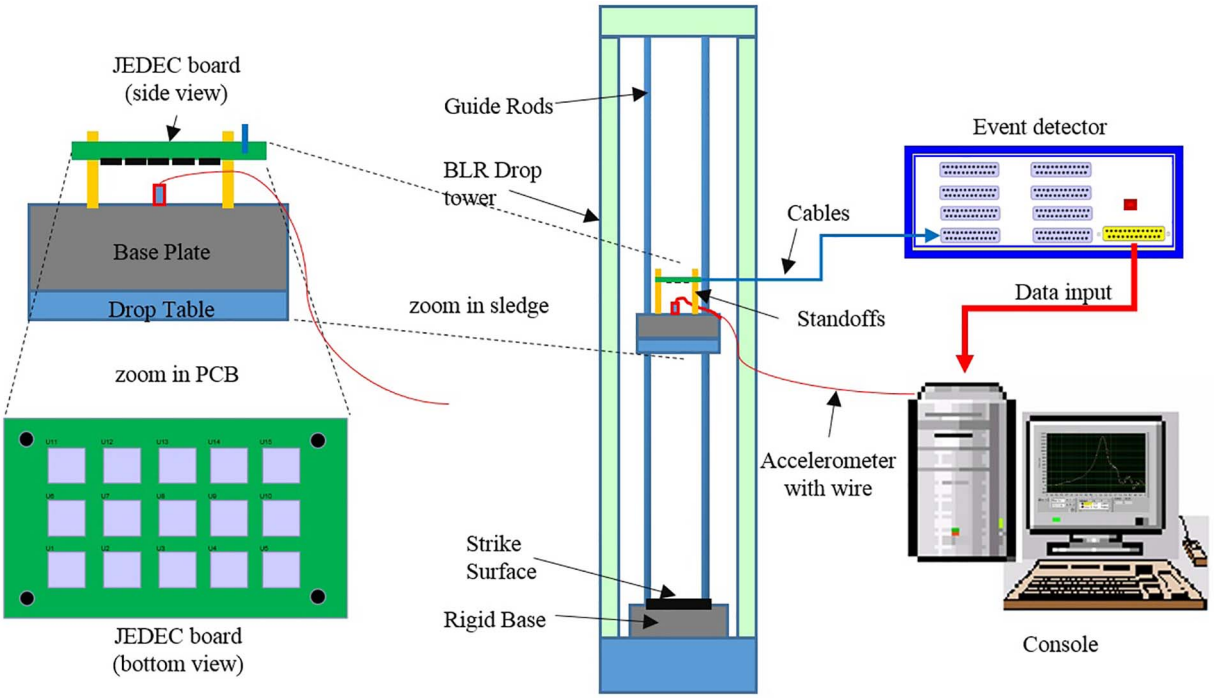

Fig. 1. BLR setup, drop tower and overall setup.

relevant between PCB and IC packages through a daisy-chained structure. Electrical failures may result from various failure modes, such as trace cracking on board, cracking of solder interconnections between the IC package and the board, and IC package cracks.

For the evaluation of product lifetime, a defect must be found to identify the failure modes using a failure analysis [6,7] for exact evidence after the BLR drop test. However, sometimes the fault location is difficult to detect precisely on a daisy-chained structure using resistance measurements. In this paper, we focus on how to apply the concept of mismatching characteristic impendence as an FA approach to detect fault locations using time-domain reflectometry (TDR) after a BLR drop test.

2. Experimental procedure

The setup of the BLR drop test follows JESD22-B111 [8]. This involves soldering cables to the plate through holes on the end of the board, mounting board on the standoffs with the package facing down, and connecting cables to the event detector. The overall board size is 132 mm × 77 mm, which can accommodate up to 15 components of the same type in a 3 row by 5 column format. The 15 components are monitored through an in-situ test using an event detector. The event detector's threshold resistance is set at 1000 Ω because any electrical discontinuity involving a resistance higher than 1000 Ω lasting for 1 microsecond or longer could be judged as a fail event. The setup of the drop test equipment is shown in Fig. 1 [8].

Before launching the BLR drop test experiment, the calibration of the apparatus on the drop table is set to be released into freefall from a specific height. During calibration, the shock pulse is measured for each drop to ensure that the input pulse remains within the specified tolerance. Adjustments are made to the drop height or replacement of the strike surface to meet the requirements. The load condition is a half sine pulse with an amplitude of 1500 Gs (standard gravity), a pulse width of 0.5 millisecond (± 10%, and a process capability index > 1.33). A lightweight accelerometer is fixed on the base plate of the component located at position U8 to characterize the output acceleration response of the PCB assembly. The shock pulse of the major waveform must be a half-sine shape. The drop tester includes a magnet catcher to eliminate rebound.

2.1. Specimen

For the sample preparation, the daisy-chained package was a Low profile Fine-pitch Ball Grid Array (LFBGA) with 160 solder balls. The solder ball uses a full matrix 96.5Sn-3.0Ag-0.5Cu (SAC305). The ball pitch was 0.8 mm, and the diameter was 0.45 mm. The package body size was 12 × 12 mm^2. There was a mechanical dummy die used inside the package to simulate the actual structure of the package. The size and thickness of the dummy die was comparable to functional dies used in applications. Both the substrate and the PCB were surface finished with Organic Solderability Preservatives (OSP) to avoid any copper oxidation before the surface mount technology (SMT) process.

This daisy-chained routing was designed to connect the solder balls placed at the packaged corners because the corner balls in