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ORIGINAL ARTICLE

New low power adders in Self Resetting Logic with Gate Diffusion Input Technique

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Abstract The objective vividly defines a new low-power and high-speed logic family; named Self Resetting Logic with Gate Diffusion Input (SRLGDI). This logic family resolves the issues in dynamic circuits like charge sharing, charge leakage, short circuit power dissipation, monotonicity requirement and low output voltage. In the proposed design structure of SRLGDI, the pull down tree is implemented with Gate Diffusion Input (GDI) with level restoration which apparently eliminated the conductance overlap between nMOS and pMOS devices, thereby reducing the short circuit power dissipation and providing High Output Voltage V_{oH}. The output stage of SRLGDI has been incorporated with an inverter to produce both true and complementary output function. The Resistance Capacitance (RC) delay model has been proposed to obtain the total delay of the circuit during precharge and evaluation phases. Using SRLGDI, the primitive cells and 3 different full adder circuits were designed and simulated in a 0.250 μm Complementary Metal Oxide Semiconductor (CMOS) process technology. The simulated result demonstrates that the proposed SRLGDI logic family is superior in terms of speed and power consumption with respect to other logic families like Dynamic logic (DY), CMOS, Self Resetting CMOS (SRCMOS) and GDI.
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1. Introduction

With continual technology scaling and improvements in lithography, the integrated system has become faster and thus it is employed in diverse real-time applications like mobile, digital signal processing, multimedia application and scientific computation. To support high-performance applications, proper choice of technology selection and topology for implementing various logic are the mandatory issues in designing low-power devices (Uma and Dhavachelven, 2012a).

The Pass Transistor Logic (PTL) (Chatzigeorgiou and Nikolaidis, 2001) circuit offers better characteristics than static CMOS. PTL can implement most functions with fewer transistor counts, thus reducing the overall capacitance, which results in faster switching times and low power dissipation. The general issue pertaining to this PTL logic is voltage variation due to threshold drop owing to series resistance between input and output. These demerits were surmounted using

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Complementary Pass-Transistor Logic (CPL) and Swing Restored Pass-Transistor Logic (SRPL) (Parameswar et al., 1994; Sasaki et al., 1996). However this logic produced larger short circuit currents, high transistor count to realize a simple gate and high wiring overhead due to the dual-rail signals.

The GDI (Morgenshtein et al., 2002; Uma and Dhavachelvan., 2012b; Agrawal et al., 2009) is the lowest power design technique, which is suitable for designing fast, low-power circuits, using reduced number of transistors (as compared to Transmission Gate and CMOS). The main drawbacks associated with GDI include: The bulk terminals are not properly biased thereby the circuit exhibits threshold drop and variation in V_t. Because of floating bulk, the cells can be implemented in SOI process which would increase the cost of the fabrication. These demerits can be overcome by permanently connecting the bulk terminals pMOS to VDD and nMOS to GND which resolves the threshold variation. This configuration provides suitability for fabricating the logic cells in CMOS p-well and n-well process. Until today static CMOS has been the design style of choice for IC designers due to its robustness against voltage scaling and transistor sizing (high noise margins) and thus the operation is reliable at low voltages (Bisdounis et al., 1998). The disadvantage of CMOS is the substantial number of large pMOS transistors, resulting in high input loads and when the operating frequency increases the circuit dissipates more power. The propagation delay is slightly higher when compared to other logic family due to its larger node capacitances.

Dynamic logic families are a good candidate for high speed and high performance circuit than the conventional static CMOS. Dynamic logic requires fewer transistors to implement a given logic function, less area and faster switching speed due to its reduced load capacitance (Yee and Sechen, 1996; Balsara and Steiss., 1996; Srivastava et al., 1998. However this circuit suffers from charge sharing, charge leakage, loss of noise immunity, timing problem due to clock input and feed through. These issues can be suppressed using an asynchronous dynamic circuit named Self Resetting CMOS (Kim, 2001). Asynchronous SRCMOS circuit operation has a separate precharge and evaluation phase which discharges the dynamic storage nodes to evaluate the desired logic function and then resetting these nodes back to their original charged state by a local feedback timing chain instead of a global clock. One of the advantages of self-resetting logic is that when the data present at the evaluation phase does not require dynamic node to discharge, which makes the precharge device inactive thereby reducing power (Litvin and Mourad, 2005; Uma, 2011. However this scheme endures from short circuit power and low output voltage due to nMOS pull down network producing conductance (direct path between) overlap between nMOS and pMOS. So the primary objective of this work focuses to resolve the problem incurred in the existing SRCMOS to support low-power and high-speed applications.

2. Various dynamic logic

The group of dynamic logic family offers good performance over traditional CMOS logic. The basic operation of dynamic logic is normally done with charging and selectively discharging capacitance. The logic operation needs two sub-cycles to complete (precharge and evaluation). During the precharge phase the clock signal charges the capacitance and during the evaluation phase the clock discharges the capacitance depending upon the condition of logic inputs.

Various dynamic logic circuits are portrayed in Fig. 1. The logic circuit in Fig. 1(a) leads to contention problem during precharge and this problem is resolved by incorporating an nMOS stack at the bottom as shown in Fig. 1(b). The demerits associated with circuit as shown in Fig. 1(c) are loss of noise immunity and a serious restriction on the inputs of the gate (monotonicity problem) and only the non-inverting logic can be implemented. These problems are surrogated using the NORA CMOS circuit as shown in Fig. 1(d). But the problem with the logic is global clock presenting clock distribution grid and routing to dynamic gates that presents a problem to CAD tools and introduces issues of delay and skew into the circuit design process. Domino logic with charge-keeper circuit has been developed to combat this problem. The circuit realization is shown in Fig. 1(e), but the demerits of the circuit are: a slow clock slope leading to conductance overlap between nMOS and pMOS devices resulting in dc power dissipation and high sensitivity to noise. An asynchronous dynamic logic self-resetting CMOS (SRCMOS) circuit technique is shown in Fig. 1(f). In this logic no global clock is required and all the operation is controlled through the inverter chain between pMOS and output. The general issue related to this logic is static power consumption and if the width of the pulses must be controlled carefully or else there may be contention between nMOS and pMOS devices, or even worst, oscillations may occur.

3. Proposed Self Resetting Logic with Gate Diffusion Input (SRLGDI)

3.1. Problem statement

Self-resetting circuitry automatically precharges themselves (i.e., reset themselves) after a prescribed delay by conditionally charging the dynamic nodes to evaluate the desired logic function using a local feedback timing chain instead of a global clock. Although this SRCMOS logic inherits lot of merits, it still suffers from static power dissipation due to the nMOS logic structure. As stated earlier, during precharge the nMOS stack is completely open and the output is fed back to the pMOS block to charge the capacitor C_y. During this period the nMOS transistors operate in cut-off region exhibiting subthreshold current. Moreover during the evaluation phase when the entire nMOS transistor in the n-block and P_{reset} transistor is ON direct impedance path exists between the VDD of P_{reset} transistor and nMOS block leading to static power dissipation. The width of the pulses must be controlled carefully or else there may be contention between nMOS and pMOS devices, or even worst, oscillations may occur. These demerits can be surmounted using GDI technique. The change done in the existing SRCMOS, instead of nMOS logic pull down tree, it is replaced by GDI logic with level restoration.

3.2. Circuit topology of SRLGDI logic

In the existing SRCMOS logic the pull-down tree is realized using nMOS block which consumes lot of static power. To surrogate this issue the proposed SRLGDI has been replaced by

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