Optik 148 (2017) 181–186

Contents lists available at ScienceDirect

Optik

journal homepage: www.elsevier.de/ijleo

Full length article

High performance gain demodulate system for hybrid fiber-coaxial

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ARTICLE INFO

Article history:
Received 30 May 2016
Received in revised form 8 August 2017
Accepted 22 August 2017

Keywords:
HFC
EPoC
QAM soft decision
Quasi-cyclic LDPC

ABSTRACT

Gigabit capable of Hybrid Fiber-Coaxial (HFC) represented an increase. The goals of the next generation HFC system are to efficiently utilize the precious last 100 m of the coaxial cable and to achieve a Gigabit transmission rate. This target demands higher requirements regarding the physical layer (PHY) throughput. Firstly, the PHY architecture of next generation HFC system is given in detail. Secondly, in order to meet challenging high PHY throughput, a class of Low Density Parity Check (LDPC) code is selected as the Forward Error Correction (FEC) scheme, the ultimate choice is made on the basis of system with a better bit error rate performance. Finally, this paper combines the characteristics of Gray code symbol mapping for Quadrature Amplitude Modulation (QAM) constellation to design a soft decision algorithm based on signal diversity. Especially in terms of power efficiency, this algorithm can beyond the performance of log-MAP algorithm.

1. Introduction

Hybrid fiber-coaxial (HFC) is a telecommunications industry term for a broadband network that combines optical fiber and coaxial cable. It has been commonly employed globally by cable television operators [1,2]. Ethernet Passive Optical Network Protocol Over Coax (EPoC)represents the development direction of the next generation HFC network, this technology provides a new end-to-end solutions to realize end-to-end management, control, scheduling, Quality of Service (QoS) and Ethernet/IP. EPoC can be widely employed in various coax scenarios of the existing HFC network. Optical Network Unit (ONU) and Coax Line Terminal (CLT) provide configuration, management and QoS from OLT to Coax Network Unit (CNU) [3,4]. With this approach, not only the fiber network development direction is satisfied, but also the coaxial cables [5], representing the precious last 100 m to the household, are efficiently utilized. LDPC code and Turbo code are two leading-edge FEC technology. Turbo code was adopted in Digital Video Broadcasting (DVB), 3rd Generation Partnership Project (3GPP) Wideband Code Division Multiple Access (W-CDMA) and Long Term Evolution (LTE) [6], LDPC was chosen for updating the downlink of DVBS2 targeting delivery of television via satellite [7]. Both were adopted by IEEE 802.16 [8]. However, PHY of HFC only needs one FEC, furthermore, high throughput must be supported. A detailed comparison of the two FEC scheme is needed. High speed transmission was based on signal mapping of high order QAM, that owing to high bandwidth efficiency.

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http://dx.doi.org/10.1016/j.ijleo.2017.08.124
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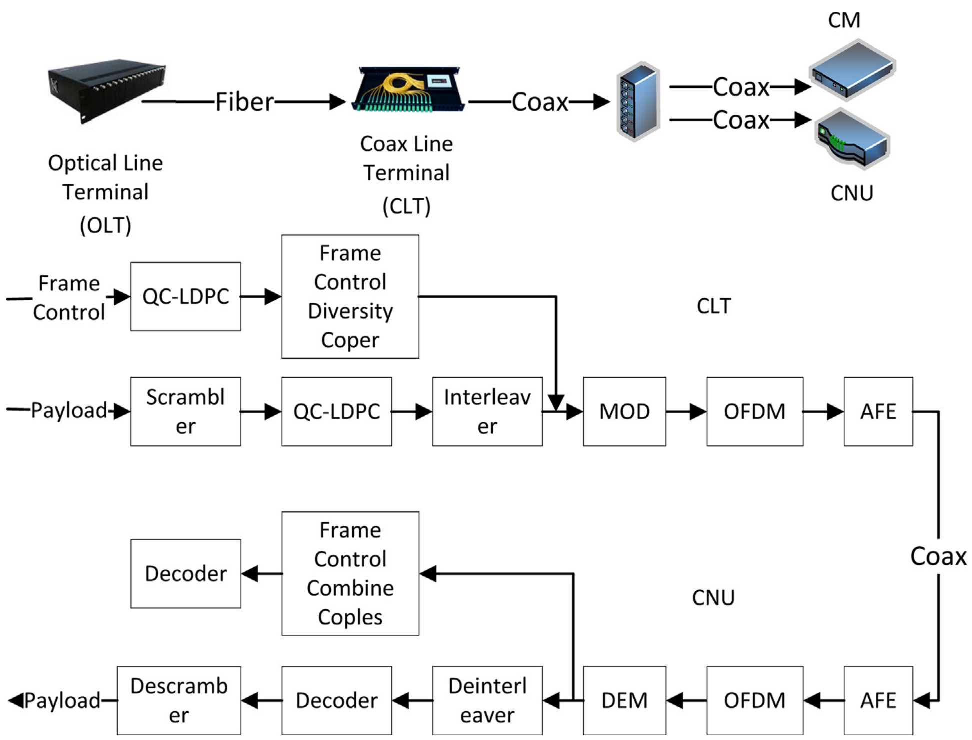

Fig. 1. EPoC topology without amplifier and PHY transceiver block diagram.

However, current soft decision algorithm is hardly break through the power efficient of log-MAP algorithm [9]. This paper proposed a div-log-MAP algorithm, which will lead to the rapid development of high order QAM modulation.

2. System architecture

Fig. 1 illustrates the relationship of CLT and CNU, and the PHY of CLT or CNU [10]. The PHY is based on bit-loaded Orthogonal Frequency Division Multiplexing (OFDM) modulation and is designed to operate as close as possible to the coaxial cable channel capacity. The basic channel support frequency band is 7.6 MHz ~ 30 MHz, the extended channel support frequency band is 65 MHz ~ 1 GHz, the single channel bandwidth is 16 MHz (8 MHz × 2), and the maximum bandwidth is 192 MHz (16 MHz × 12). The extended bandwidth provides PHY rate of 1 Gbps, and the basic bandwidth and the extended channel provide a 2.4 Gbps PHY rate. Examining the data path details in the block diagram, it is observed that at the transmitter side, the PHY layer receives its inputs from the MAC layer. Two separate processing chains are shown because of the different encoding. Frame control data are processed by the frame control encoder, which has a FEC encoder and frame control diversity copier, while the payload data stream passes through a scrambler, a FEC encoder, and an interleaver. The QAM mapper, the pilot signal insertion, the inverse fast Fourier transform processors, the preamble and cyclic prefix insertion, and the symbol window and overlap blocks eventually feed the Analog Front-End (AFE) module with one of the ports that couple the signal to the coax medium. At the receiver, an AFE with one receive port operates with individual Automatic Gain Control (AGC) modules and one time-synchronization, through an equalizer and QAM de-modulator, to feed separate frame control and payload data recovery circuits, and a de-scrambler to recover the payload data.

3. FEC

LDPC code and Turbo code are two leading-edge FEC technology [11]. The LDPC is a high-performance code that nearly approaches the Shannon limit. The property of being without an error floor makes it suitable as the FEC scheme for EPoC, Ethernet over Coax (EoC) or Power Line Communication (PLC).

Fig. 2 shows that the BER performance in Additive White Gaussian Noise (AWGN) channel and Binary Phase Shift Keying (BPSK) modulation for both the LDPC code with the code word is 8190 bit, the code rate is 1/2, and that for the turbo code with the code word is 2046 and 8190 bits (with tail), the code rates are 1/2 and 1/3, the generators are 05 and 07, and the constraint length is $K=3$. K is often called the depth, the output is a function of the current input as well as the previous K-1 inputs. For the low SNRs region, the error probability changes very slowly as a function of E_b/N_0, whereas for the moderate SNRs region, the error probability decreases rapidly with increasing E_b/N_0. The latter region is the turbo cliff region. Finally, for moderately large E_b/N_0 values, the code exhibits an error floor, which is typically achieved with a few iterations. The