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High reliability reconfigurable FOG signal processing system for satellite

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ABSTRACT

This paper focuses on accomplishing the high reliability reconfigurable FOG signal processing system. Design is done to improve the reliability of the entire system. In order to realize the system reconfigurable, SRAM-based FPGA is adopted as the signal processor. Scrubbing technology based on active partial reconfiguration is used to insure the SRAM-based FPGA operating properly. A 14 MeV neutron radiation experiment is taken to evaluate the radiosensitivity of the system. It is concluded that the design with scrubbing technology as core can increase the reliability significantly. This lies the foundations for the application of high reliability reconfigurable FOG for satellite.

1. Introduction

FOG (fiber optic gyroscope) technology has proved its capacity to adapt to a great variety of environments, from deep blue sea to space. FOG has particular advantages for space application and satellite attitude and heading control: the main one being its high reliability as a solid state technology with no moving parts subjected to weariness. It is oriented toward high and very high performance, it can measure very low rotation rate; arbitrarily low angular resolution, it presents good behavior under vacuum and radiation. Moreover, the intrinsic sensitivity to thermal transient and to vibrations are not that important on satellites that have often a good thermal control and very quiet mechanical environment in orbit [1]. The signal processing system is one of the most important parts of FOG. Antifuse FPGA is always used as the controller of the signal processing system for FOG used in space.

Recently, more and more institutes and space organization have applied reconfigurable technology on space electronics design. In some applications, FOG is asked to be reconfigurated for updating or multi-purpose. Because SRAM-base FPGA is capable to be reprogrammed an unlimited number of times, even in the end-user system, it is used as the signal processor for some reconfigurable FOG. However, SRAM-based FPGAs are sensitive to the space radiation environment, particularly radiation induced single-event upset (SEU) and single-event latch (SEL), caused by high energy ions, protons, neutrons, etc. In SRAM-based FPGAs, the configuration of the design mapped into the FPGA chip is stored in SRAM cells, which specify the functionality of the circuit mapped into the FPGA. A particle hit on memory resources causes a error in the mapped design. The error caused by SEU and SEL may lead to data corruption and system crashing. For these reasons, the safe use of SRAM-based FPGAs in space requires careful design considerations. Conventional fault-tolerant schemes try to protect the design by using either spatial or temporal redundancy. There are two major types of memory resources in FPGAs, user bits and configuration bits. One of the most common mechanism to protect both configuration and user bits is the triple modular redundancy (TMR) scheme in all used logic and routing resources [2,3]. TMR-based SEU mitigation techniques

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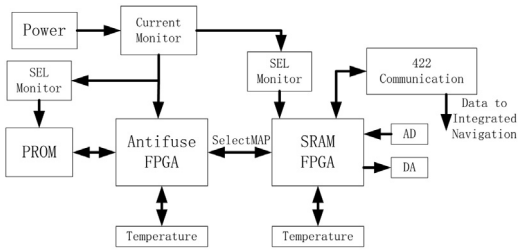

Fig. 1. System structure.

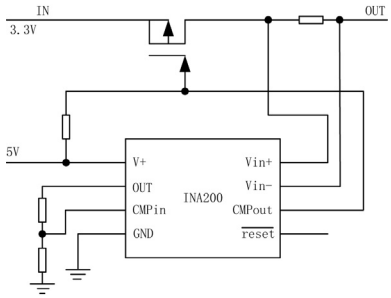

Fig. 2. SEL monitor circuit.

impose more than 200% overhead in terms of area and power [4,5]. However, the design of FOG for space must achieve the ultimate goal, which is to make reasonable balance of reliability, power consumption, and performance. Therefore, with the reconfiguration ability of SRAM-based FPGA, scrubbing technology is proposed to improve the reliability of reconfigurable FOG for space.

In this paper, we present information on design of high reliability reconfigurable FOG signal processing system for satellite. In the reset of the paper, Section 2 presents the design of the system for processing. Section 3 describes the scrubbing technology for improving the reliability. Section 4 provides the experiment to prove the method available. Lastly, Section 5 presents our conclusions.

2. System design

In connection to application-specific high reliability reconfigurable FOG, SRAM-based FPGA, which is sensitive to single event upset, has to come in as the signal processor to achieve the reconfigurability. In such a case, necessary measures must be applied to improve the reliability of the system. From a system view, there are five major parts that constitute the entire signal processing system: (1) SEU mitigation for SRAM-based FPGA, (2) monitor to SEL induced overcurrent for radiation sensitive device, (3) safeguard for power supplied to the system, (4) temperature monitor to the system, (5) communication link for integrated navigation. To illustrate, the structure of the system is shown in Fig. 1.

The program of the signal processor, SRAM-based FPGA, is stored in the PROM, as shown in Fig. 1. To decrease the accumulation of SEU in the SRAM-based FPGA, an Antifuse FPGA, which is insensitive to SEU, is adopted to control the scrubbing to the SRAM-based FPGA. Both of the two FPGAs are connected in SelectMAP mode. When system electrified, the signal processing program from PROM are configurated into the SRAM-based FPGA through the Antifuse FPGA. Then, the signal processing system goes into operation. The PROM connects to the Antifuse FPGA through parallel mode. For the record, the Antifuse FPGA is just used to implement the initial configuration and scrubbing to the SRAM-based FPGA.

Because the power consumption and current would increase quickly when the radiation sensitive devices are subject to SEL, the current must be shut down as soon as possible in order to avoid the damage of the devices. In the design of the system, a SEL monitor circuit is designed to real-time monitor the current of the SRAM-based FPGA and PROM, and implements overcurrent protection of them. The design of the SEL monitor circuit is illustrated in Fig. 2.

At power starting instant, surge current may happen in the system power current. When one of the devices in the system has got trouble, the system power current may overload. In order to improve the reliability of the system, a current monitor circuit is designed to implement overcurrent protection to the system. AAT4610 is adopted as the core chip to real-time monitor the current.

In the system, two TMP100 chips are used to real-time monitor the working status of the system as the temperature sensor. The temperature information collected by the chips is sent to the SRAM-based FPGA and the Antifuse FPGA.

The communication module, as shown in Fig. 1, consists of RS-422 protocol chip DS36F95. It is used to convey the palstance data and temperature information to the navigation solution system.