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Encoder Improvement for Simple Amplitude Fully Parallel Classifiers Based on Grey Codes

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Abstract

The present article describes functionality of real-time classifier usable for data flow statistical parameters calculations, different modulation types symbol detecting and in other applications, where the fastest association of input signals sample is required with one of the predefined categories. The effective implementation of encoder with high number of bits for fully parallel classifier is provided based on Gray codes (Gray, 1953). The work is concluded with comparative analysis of encoder standard implementation and its optimized version for FPGAs manufactured by Xilinx and Altera companies.

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1. Introduction

The problem of high speed data processing gains its actuality with wide spreading of embedded control/monitoring systems for physical world processes (PWP), which leads to:

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- increased complexity of implemented algorithms (i.e., it is possible to implement more complex processing algorithm with higher data rate and same time interval, since PWP wasn't altered);
- development of new application fields (i.e., increase of performance allows former algorithm to be used in such areas, where it couldn't be applied before, since implementation environment was lagging behind PWP).

Another factor leading to more complex algorithm is information volume increase, since improvement of algorithm structure makes it possible to process higher volumes of data.

That is why programmable logical devices (PLD) are getting increasingly popular for solutions in fast processing and/or operating with high volumes of data. The main advantage of PLD in specified field is a possibility to implement complex parallel algorithms with performance improvement by Bashkirov and Muratov (2012) compared to serial algorithms implemented in standard processing devices. The following facts confirm the foregoing:

- Intel corporation added Field Programmable Gate Array (FPGA) structures into latest server processors Xeon according to Shah (2016);
- FPGA devices are used in Microsoft Corporation datacenters to speed-up data processing, in particular, performance gain in case of Bing search engine is 95% according to Putnam (2014);
- the further development of this idea in Microsoft Corporation leads to research of FPGA applications in neural networks (Deep Convolutional Neural Networks) for performance improvement according to Ovtcharov (2015);
- FPGA devices are used for search of dark matter in CHIME telescope by Leibson (2014) to split digitized data into 1024 frequency channels from 16 analog-to-digital convertors (ADC) with transfer rate of 15.5 Gbps;
- Mango Communications in cooperation with Rice University developed system for 802.11s standard wireless system dynamics real-time research, which uses 24 FPGA devices connected to 96 antennas by Murphy and Zhong (2014).

One of the most important objectives of information processing algorithms is execution of specific procedures over objects according to their affiliation to some groups with specified properties. Such tasks can be found in multiple fields:

- in communications: analog-digital conversions, symbol detectors of various modulation types, enhancement of calculation consuming functions tabular implementation;
- big data & statistics: histogram construction, frequency analysis of text data arrays;
- computer vision (theory of objects recognition): calculation of similarities between objects, partitioning of objects set into separate groups;
- networking technologies: users distributions in priority groups, for example based on their activity results;
- automated trading systems: filtering the most profitable orders and hiding the unfavorable deals;
- neural networks: making decision at output of neuron, finding greatest weight in neural network;
- hardware implementation of cryptographical algorithms: privacy-preserving classification;
- and other.

Such type of applications will be further referred to as processing with pre-classification of objects. To improve performance of entire system it is desirable to merge these two operations (classification and processing).

If classification implies distribution of objects interpreted by numbers into groups based on their values (amplitudes), then such task can be solved by device further in text referred to as simple amplitude classifier (SAC).

2. Taxonomy of simple amplitude classifiers

SAC implementation variations are shown in Fig. 1. Let's describe advantages and shortcomings of these methods with special accent on FPGA implementation due to effective capabilities for high speed data processing on this platform.