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Ultraviolet Laser Diode Ablation Process for CMOS 45 nm Copper Low-K Semiconductor Wafer

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Abstract

This paper presents the optimization work of 355 nm ultraviolet (UV) laser diode ablation process for CMOS 45 nm Copper (Cu) low-k semiconductor wafer. The micromachining parameters included laser power, laser frequency, feed speed, and defocus amount were optimized via design of experiment (DOE). Package reliability stressing tests were carried out as part of the efforts to validate the robustness. The results show that high repetition rate, low laser pulse energy and a high pulse overlap produced zero dicing defects. The laser groove depth increased as the laser pulse energy increased. It is shown that, laser grooving is one of the best solutions to choose for dicing quality, throughput and yield improvements for CMOS 45 nm Cu low-k wafer dicing.

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Keywords: Advanced dicing tehcnology; Laser micromachining, laser ablation, laser grooving, laser scribing, laser dicing, ultra low-k, semicoonductor wafer

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1. Introduction

Silicon wafer is brittle and hard in nature, metal layers peeling, chipping, cracking and delamination are the most common dicing defects produced by diamond blade dicing. Diamond blade dicing is a process to get every single IC chip separated from a semiconductor wafer. Hair-line defect from diamond blade dicing is difficult to be detected as it is hidden beneath the top wafer surface. The micro crack initiated during the diamond blade dicing, and the cracks may have propagated towards the die circuitry area from the die edge, resulting in die-level interconnections failures [1-2]. In semiconductor industry, the current trend is to use Cu low-k and ULK dielectric film in the wafer fabrication process for better electrical, mechanical and thermal performance. The aluminium (Al) metal interconnects will be replaced by Cu and the traditional silicon dioxide (SiO_2) will be replaced by Cu low-k and ULK dielectric materials. Chaware et al. have studied a model of laser dicing for 90 nm Cu low-k bumped wafer. It was using a combined laser and blade dicing process. Good and promising dicing responses were reported [3].

To achieve a defect-free dicing process, specifically for Cu low-k / ULK wafers, laser dicing technology has been brought out due to its promising dicing responses over the conventional blade dicing technique. The principle of laser dicing is using the focused laser light onto the Si wafer by using a condenser lens to cause ablation. When the laser light is irradiated on a Si wafer, and the intensity of the laser light is over the threshold, the light is converted into electrical, thermal, photochemical, and mechanical energy. It follows that a neutral atom, molecule, positive and negative ion, radical, cluster, electron and light are released explosively and the surface of the Si wafer is etched [4-6]. Unlike the laser ablation processing normally used in laser machining, no Si or top-layer debris is produced on the device surface. Also, there is none of the residual stress that occurs on the laser incident face or the back of the wafer accompanying heat shock when ablation processing is used.

The purpose of this research is to establish the optimization work of 355 nm ultraviolet (UV) laser diode ablation process for CMOS 45 nm Copper (Cu) low-k semiconductor wafer. Unlike the conventional diamond blade dicing, laser dicing is possibly one of the potential solutions to overcome the dicing quality, throughputs, and yield issues.

2. Methodology

2.1 Wafer selection

A 9 x 9 mm Encino dicing-specific test vehicle die was used in this study. It was fabricated via CMOS 45 nm Cu low-k technology with 10 Cu layers and 2.1 µm aluminium (Al) pad thickness. The wafer diameter and die thickness used in these experiments are 300 mm and 280 µm respectively. The saw street width evaluated in the test vehicle was 120 µm. The basic wafer information is recorded in Table 1.

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