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An induction machine and power electronic test system on a field-programmable gate array

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Highlights

- We present induction machine model for FPGA simulation, suitable for Hardware-In-the-Loop tests.
- We present a novel variable parameter and variable topology FPGA circuit simulation solver.
- We also present other available motor (PMSM and SRM) on FPGA.
- All models and solvers are made in IEEE floating-point format and a unique FPGA bitstream is required.

Abstract

This paper presents a field-programmable gate array (FPGA) test system composed of an induction machine, configurable as a doubly-fed induction machine or squirrel-cage induction machine, with power electronic converter models suitable for virtual motor drive control development and testing. The IM model is designed so that all parameters can be modified online without stopping the simulation. The power electronic part is customizable using a variable topology FPGA solver called Electric Hardware Solver (eHS). Permanent magnet synchronous machine and switched reluctance motor drive FPGA models are also discussed. The system is designed for fast design iteration process by allowing circuit and parameter modification using a unique bitstream. The system allows control engineers to validate production controllers in real-time, using virtual motor drives. The paper also briefly explains permanent magnet synchronous motor drives and switched reluctance motor drive implementations on FPGA.

Keywords: Induction motor drive; Hardware-In-the-Loop simulation; eFPGAsim; Permanent magnet synchronous motor (PMSM) drive; Switched reluctance motor (RSM) drive

1. Introduction

The use of Field-Programmable Gate Array (FPGA) devices for the purpose of real-time simulation is an emerging trend for the Hardware-In-the-Loop (HIL) simulation. FPGA-based HIL is especially well adapted for high frequency PWM motor drives and power converters due to their very high sampling frequencies, typically in the nanoseconds range. HIL techniques are used for various applications [4] with the main objective of decreasing time-to-market of

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increasingly complex control systems and keeping the budget impact at bearable levels during the development phase, while running realistic tests in a safe environment using the actual controller hardware. The computational speed of FPGA, combined with their fast coupling capability with I/Os make them an excellent choice for such applications. In particular, FPGA-based models exhibit a very low HIL loop latency, sometimes a critical aspect in some high-end motor controller and protection system tests during normal and fault conditions.

Induction motor HIL simulation on FPGA is explained in the literature [2,1,11,10] using either fixed-point or floating-point format. A key aspect of HIL systems, in terms of industrial usability, is the ability to easily change model parameters and circuit topology. On FPGAs, this poses a serious challenge due to the long bitstream generation times.

In this paper, we present an FPGA test system composed of an induction machine (IM) along with power electronic converter models suitable for virtual motor drive control development. The IM model is designed so that all parameters can be modified online. The power electronic part is customizable using a variable topology FPGA solver called Electric Hardware Solver (eHS) [7]. Other FPGA configurations, with permanent magnet synchronous machine (PMSM) and switched-reluctance motor (SRM), are also briefly described.

The HIL system is designed for fast design iteration process by allowing circuit and parameter modification with a single bitstream. Both eHS and the IM are designed using floating-point arithmetic. The system allows control engineers to validate production controllers in real-time using a virtual drive, including the IM (and similarly for SRM and PMSM), with the connected power electronics converter.

2. Description of the eFPGAsim suite of FPGA models and solvers

The RT-LAB real-time simulator is designed to run models on FPGA and CPU. On the CPU, most Simulink models and toolboxes like SimPowerSystems are supported. On the FPGA, a customized suite of models and solvers was designed by OPAL-RT and is called e*FPGA*sim.

In e*FPGA*sim, the set of FPGA motors and inverter models available in 2015 are:

(1) FEA-based Permanent Magnet Synchronous Motor (PMSM, IPM) [8,9].
(2) Switched Reluctance Motor (SRM) [5].
(3) Induction motor or induction generator (IM) [6].

FEA-based PMSM can simulate details such as cogging torque and saturation. Also available are more standard Linear DQ and Variable DQ (VDQ) PMSM models. VDQ is a DQ model that takes into account the saturation for all steady-state operating points. (By comparison, FEA-PMSM can handle transient saturation.) Also note that PMSM covers special cases, such as BLDC (constant inductance matrix and/or trapezoidal flux) and Interior-Permanent-Magnet (IPM).

At the center of e*FPGA*sim is the Electric Hardware Solver (eHS), a general purpose electric system solver that can be configured to simulate user defined power electronic circuits without reflashing the FPGA card. Also available in e*FPGA*sim are many types of custom-built converters, such as standard 2-level buck, boost, H-bridge buck–boost, and SRM unidirectional converters.

The e*FPGA*sim suite also allows the user to add custom VHDL or Xilinx System Generator code. These models' availability, as well as their connections, are customizable on a fixed FPGA bitstream that does not need to be recompiled. This e*FPGA*sim structure is depicted in Fig. 1.

These models are all designed *with floating-point arithmetic* and the ability to change all parameters on-line. All these models have a sampling times below 500 ns and a total HIL latency close to 1 μs. Latency is defined here as the delay from the IGBT gate capture to the corresponding effect on the motor current at the analog output of the simulator. In essence, e*FPGA*sim is a set of precompiled modules, including eHS, that come in different configurations. Each configuration is a unique bitstream in which connections and parameters can be changed.

The availability of the induction machine in e*FPGA*sim was first described in [6]. In the next section, section, we describe the equations of the induction machine used in the e*FPGA*sim implementation; common e*FPGA*sim configurations involving PMSM and SRM are discussed in Section 5. Note that these configurations can be modified according to special requirements. Typically, a configuration comes with a user-chosen set of models and solvers that can be configured and inter-connected by the user.