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Study on mobile hole generation in blend MoO_3:CuPc by capacitance-voltage method

A.R. Yu, Y. Pei, R.C. Yi, S.B. Liu, M. Chu, H.M. Yu, Y.J. Tang, Z.S. He, X.Y. Hou*

State Key Laboratory of Surface Physics, Key Laboratory of Micro and Nano Photonic Structures (Ministry of Education), Collaborative Innovation Center of Advanced Microstructures, Fudan University, Shanghai 200433, China

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ABSTRACT

Systematic C-V measurements were carried out on specially designed capacitance-like devices to study the generation of mobile carriers in 1:1 v% MoO_3:CuPc blend layer. In these devices, it was experimentally found that only mobile holes were generated by the external electrical field. These mobile holes were generated from CuPc molecules and could only transport among them. Based on this hole generation mechanism, all the enhancements of hole transport in CuPc layer reported previously could be explained by the extra mobile holes generated in the blend, increasing conductivity. Meanwhile a model of capacitance with mobile carriers has been proposed, and the relation between the amount of mobile holes generated and the applied bias voltage has been calculated accordingly. Quite reasonable results were obtained.

1. Introduction

Owing to relatively lower carrier mobility and carrier density, the conductivity of organic small molecular semiconductors is much poorer than their traditional inorganic counterparts [1,2]. Such an inferiority might hinder the large-scale commercial application of promising organic small molecular materials in electronics field. Thus, a great deal of effort has been made to improve the conductivity of organic small molecular materials [3–13]. In recent years, P-type doping of organic materials with transition metal oxides (TMOs) has drawn much attention since devices with doped organic layer showed lower threshold voltage and enhanced power efficiency in organic light emitting diodes (OLEDs), and higher photocurrent in organic photovoltaics (OPVs) [5–13]. Among them, MoO_3 doped copper phthalocyanine (CuPc) looks ideal for hole transport and the underlying mechanism has been extensively studied [8,9,13]. Guan et al. found that MoO_3-doped CuPc layer as hole injection layer (HIL) could effectively improve the performance of OLED, and charge-transfer (CT) complex between CuPc and MoO_3 molecules was confirmed by peak red shift of UV–visible spectra [8]. They believed this CT complex played decisive role in improving the performance. Additionally, they improved the stability of CuPc/C_{60} based OPV with same blend and believed that improved hole transport of MoO_3 doped CuPc played positive role as well [9]. However they didn't show the reason of the improvement of hole transport by CT complexes. Ke et al. studied the interface between MoO_3 and CuPc, UV–Vis absorption and XPS measurement revealed that electrons transferred from CuPc molecules to MoO_3 molecules [10]. Similar results on MoO_3/CuPc interface had also been obtained by Wang et al. with UPS measurement [11] and Irfan et al. with AR-XPS study [12]. Their studies provided clear transfer direction of electrons, *i.e.* from CuPc molecule to MoO_3 molecule. Although this electron transfer is generally accepted, how this charge transfer improved conductivity is still a question open. On the contrary, Qiao et al. considered hole hopping transport along MoO_3 sites as the main conduction mechanism in MoO_3-doped organic films, rather than charge transfer between MoO_3 and organic molecules [13]. Up to now, the mechanism of the enhanced transport in MoO_3 doped CuPc is still controversial [8,9,13], although the majority believe that CT complex is crucial, whether mobile carriers are really generated has never been verified experimentally, not to mention the polarity of mobile carriers and their amount.

Recently, the authors conducted systematic capacitance-voltage (C-V) measurements on a series of specially designed capacitance-like devices with blend MoO_3:CuPc as generation layer of mobile carriers, and experimentally confirmed that only mobile holes were generated in 1:1 v% MoO_3:CuPc blend. The mobile holes from CT

* Corresponding author.
E-mail address: xyhou@fudan.edu.cn (X.Y. Hou).

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complex between MoO_3 and CuPc molecules were generated by external electrical field. The mobile holes were generated in CuPc molecules, and could only transport among them. Moreover, the variation of the amount of mobile holes with applied bias was calculated based on the measured C-V curves and quite reasonable results were obtained.

2. Experimental details

Each layer of the device studied was deposited by vacuum thermal evaporation with chamber pressure maintained below 10^{-4} Pa. The deposition rate was 3 Å/s for Al and 0.5 to 1 Å/s for other materials. All materials and ITO substrates were commercially purchased without further treatment. Through a shadow mask, a sample with 3 mm × 3 mm effective area was formed. C-V measurements with parallel mode were conducted in dark by a Keithley 4200 Semiconductor Characterization System with 4210-CVU, and AC signal was set as 1 kHz, 50 mV [14]. In this condition, the argument of impedance measured kept around −90°, implying nearly pure capacitance-like devices. Forward bias is defined as positive potential of the ITO/Al (3 nm) anode.

The structure of capacitance-like devices studied is shown in Fig. 1 **(a)**. A 3 nm Al layer was deposited on transport conducting indium-tin-oxide (ITO) substrates to efficiently modify the ITO work function in order to form symmetric electrodes [14]. Since sufficient carriers injected might lead to capacitance increase under bias [15], it is quite crucial to exclude the interference of such injected carriers in C-V measurement. Extensive experimental investigations showed superior double-layer insulator of 50 nm 4,4-bis[N-(1-naphthyl)-N-phenyl-amino] biphenyl (NPB) layer combined with 50 nm bathophenanthroline (Bphen) layer could effectively prevent the carrier injection. The current was no more than 200 nA under 30 V bias of either polarity for all devices. The energy potential barrier for electron injection from Al to NPB is 1.7 eV and that for hole injection is 1.3 eV [16], both are high enough. As will be stated below, only mobile holes generated in function layer, they can be well blocked by 50-nm-thick Bphen layer [17–19] and confined in the function layer. Function layers of different thickness from 50 to 90 nm thick were inserted between two insulators for carrier generation and transport. Therefore five different kinds of devices were fabricated, named as **Device A**, **Device B**, **Device C**, **Device D** and **Device E**, respectively. If mobile carriers of both polarities existed in function layer and were spatially separated by external electrical field, similarly to the case in dielectric material, the additional electrical field produced by mobile carriers would be just opposite to the externally applied one, leading to capacitance increase. Therefore, capacitance change under bias can provide plenty of information about mobile carriers and their transport.

3. Results and discussion

Since steady capacitance measurement is really sensitive to carrier generation and separation [14,15,20,21], with this easy-conducted method the polarity and amount of mobile carriers could be really determined. The C-V measurement results of **Device A** through **E** are shown in Fig. 2. The function layer is 90 nm CuPc layer in **Device A**, 90 nm MoO_3 layer in **Device B**, 10 nm blend layer + 80 nm CuPc layer in **Device C**, 80 nm CuPc layer + 10 nm blend layer in **Device D** and 80 nm MoO_3 layer + 10 nm blend layer in **Device E**. In the above, the layer before plus sign (+) means it was deposited near ITO/Al. The composition of blend layer was fixed at 50 v% MoO_3 co-evaporated with 50 v% CuPc for all devices.

In Fig. 2, the capacitance of **Devices A** (90 nm CuPc, magenta up-triangle) and **B** (90 nm MoO_3, olive down-triangle) kept almost constant of 0.579 nF and 0.685 nF respectively, throughout C-V scan from −30 V to 30 V. As discussed above, it was clear that neither intrinsic free carriers [14,15] nor generated mobile carriers could be observed in pure CuPc, MoO_3, NPB and Bphen layers. Otherwise mobile carriers would be spatially separated by applied electrical field and capacitance would increase under sufficient bias voltage. Since there was no contribution of spatially mobile carriers in **Device A** and **B**, the electrical field in function layer must be simply produced by the charge accumulated at both electrode interfaces from power supply, hence the measured capacitance must be equal

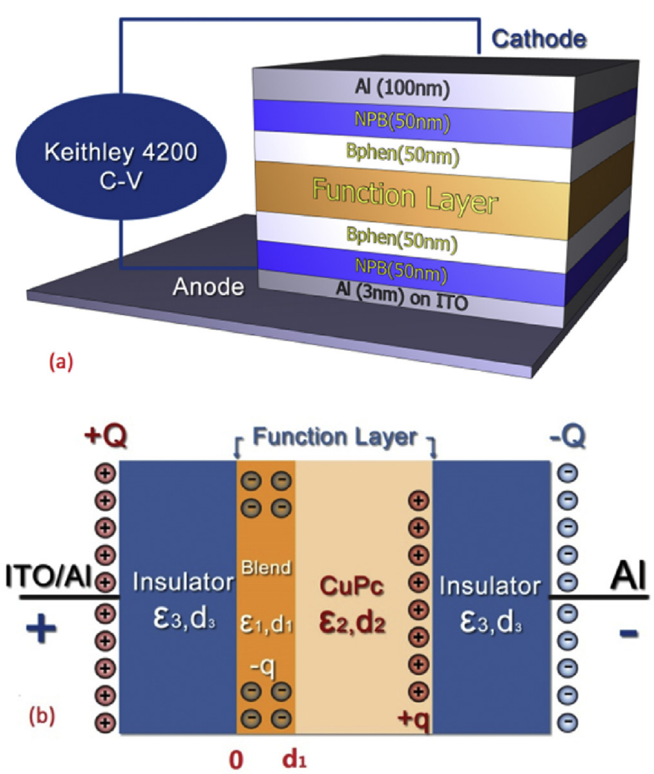

Fig. 1. **(a)** Schematic structure of capacitance-like devices; **(b)** sketch of carrier distribution in **Device C** (10 nm blend+80 nm CuPc as function layer).

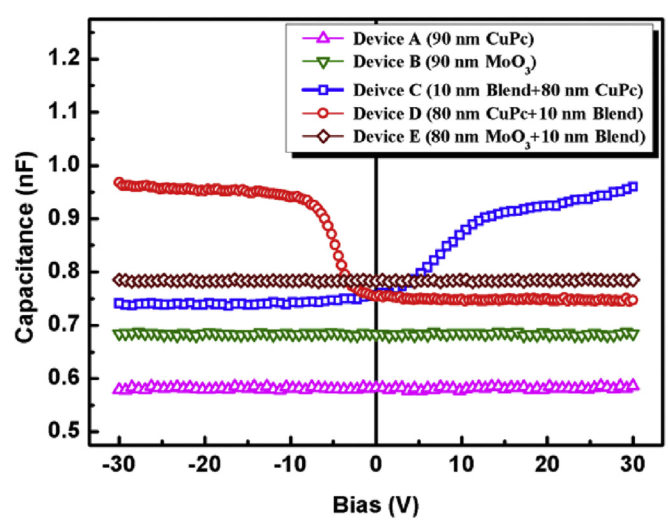

Fig. 2. C-V curves of **Device A** to **E**.