



Electric field induced ferroelectric-surface modification for high mobility organic field effect transistors



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ABSTRACT

Inherent spontaneous polarization in ferroelectric-dielectric polymer PVDF-TrFE (Poly[(vinylidene fluoride-co-trifluoroethylene)]) and an external electric field induced surface modification procedure are utilized to enhance organic field effect transistor (OFET) characteristics. The increase in the carrier mobility of the electric-field (EF) treated device correlates with the EF magnitude and evolution of dielectric microstructure and exhibits an enhancement beyond 300%. The enhanced interfacial transport property appears to have its origin in the dipolar orientation and nanostructure evolution at the interface.

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1. Introduction

Multifunctional ferroelectric materials have been used for fundamental studies and implementation of innovative devices [1]. Electro-mechanical relationship in these kinds of materials finds application in actuator, ultrasonic motors, transducers, and wearable electronics. Advent of ferroelectric polymers in organic electronics has opened up additional option to control surfaces and interfaces for fine tuning the molecular, structural and device engineering aspects [2–4]. Optimally designed and synthesized charge transport molecules for field effect transistor (FET) devices are not necessarily translated to the expected performance levels. The assembly and organization of the transporting molecule are dependent on various processing methods which are utilized during device fabrication. Some of these procedures include judicious choice of dielectric layer [5], interface treatment [6] such as thermal and siloxane exposure which minimizes defects and enhances adhesion, self assembly [7] and using low contact-resistance electrode [8]. Recent efforts to yield highly ordered structures of semiconducting polymers formed from solution phase utilize nanogrooves and prepatterned surfaces which is conducive for translating order to result in mobility as high as $19.3 \text{ cm}^2/\text{V-s}$ [9]. An order of higher density of states (DOS) in the parallel direction to

the nanogrooves compared to perpendicular direction [10] improve the charge transport. We introduce an additional novel pattern-free method in the fabrication of efficient OFETs well suited to solution process to further enhance the device properties. This strategy involves electrostatic modification of the semicrystalline dielectric (ferroelectric) substrate, to enable a higher degree of order for the deposited semiconductor in the bottom gate OFET structure.

A decisive factor in OFET performance arises from the organization of the charge transport layer at the semiconductor-dielectric interface [11–13]. An appropriate pair of dielectric and semiconductor which results in optimum surface microstructure can significantly enhance FET characteristics [14–16]. Polyvinylidene fluoride (PVDF) and its copolymers are class of dielectrics which has been explored for its ferroelectric functionalities, and are known to exhibit polymorphism during the film-treatment stages [17]. The incorporation of TrFE (Trifluoroethylene, -CF₂-CHF-) results in high crystallinity of PVDF copolymers [18,19]. Increased crystallinity of PVDF-TrFE copolymers in turn translates to higher ferroelectric and piezoelectric responses [20,21]. The high internal polarization provided by PVDF-TrFE offers an excellent template for field assisted response [22], in spite of the mild roughness introduced by the inhomogeneity of the crystalline and amorphous domains. It has been observed that semiconducting polymers such as P3HT (Poly(3-hexylthiophene-2,5-diyl)) can form ordered layers on these ferroelectric film surfaces [23]. Use of external electric field for aligning and patterning the polymer substrate has been a useful approach [24,25]. We utilize dielectric surfaces and their ability to

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reorganize under the influence of external field and offer a platform for depositing ordered semiconducting polymer films.

Charge carrier transport in solution-processed conjugated polymer FETs is largely controlled by the interfacial microstructure [13]. The molecular organization and assembly [26] formed by the semiconducting-macromolecular system play a key role and it has been shown that transport plane aligned to the molecular dipole orientation leads to higher FET mobility [27]. In this context, patterned dielectrics have been engineered as templates for the charge transport layer. Among many interfacial phenomena, forced orientation and the resulting symmetry breaking of polar molecules are important in the view of dielectric physics of these substrates [1–28]. These substrates form a template for limited epitaxial growth of polymers on them. PVDF-TrFE film surface offers a microstructure with distribution of phases, which can be systematically tracked [29,30]. We demonstrate subtle-controlled changes of this dielectric surface microstructure via a lateral electric field. Even though, the mobility value of the assembled semiconducting polymers are not extraordinarily high, the results present a direct evidence of correlation of dielectric surface-structure and OFET performance.

2. Materials and methods

2.1. Device fabrication

Semiconducting polymers PBTOR from Polyera Corporation and P3HT from American Dye Source were used in the device fabrication. PVDF-TrFE (75/25) copolymer pellets procured from Sigma Aldrich was used as the dielectric in OFET. Top contact-Bottom gate OFETs (TC-BG OFETs) were fabricated on cleaned and treated glass substrates. 40 nm Chromium-Gold (Cr-Au) gate electrodes were thermally evaporated on to the cleaned glass substrates at 4×10^{-6} mbar pressure. Shadow masks of pre-defined sizes were utilized to get desired width for the gate electrode contact. PVDF-TrFE (70:30) solution (80 mg/ml) in DMF (*N,N*-Dimethyl formamide) was spin coated at 1500 rpm for 60 s, in N_2 filled glove box. The dielectric layer coated substrates were annealed in glove box at 145 °C for 1(1/2) hour under the presence of a constant voltage bias using poling electrodes (aluminum electrode, thickness ~ 200 nm), which were thermally evaporated (orthogonal to the gate electrodes with even spacing on both sides of the gate electrode). The semiconducting polymers PBTOR (poly 4,4'-dialkoxy-5,5'-bithiazole (BtzOR)) or P3HT used for these studies, were immediately coated on the modified dielectric layer. Solution of PBTOR in Chlorobenzene (6 mg/ml) was spin coated on dielectric at 800 rpm and annealed at 90 °C for 30 min, in the N_2 glove box. Gold source drain contacts were evaporated at 4×10^{-6} mbar pressure using shadow mask to create a channel of length~40–80 μm and width ~ 1–2 mm. Source-drain masks were aligned so as to achieve minimal overlap of top and bottom contacts. It was ensured that devices were fabricated using masks of predefined dimension for electrodes to minimise the overlap between gate and source drain so as to achieve low leakage currents and parasitic capacitance (image of a typical transistor geometry and dimensions are shown in Supplementary Material Fig. S1).

2.2. Device characterization

OFET measurements were performed in vacuum chamber (10^{-3} mbar). It was ensured that the presence of the poling electrodes did not alter the typical OFET and leakage characteristics. Output and transconductance measurements on OFETs are performed using Keithley SCS-4200 while keeping the device at 10^{-3} mbar pressure. Atomic force microscopy (AFM) measurements

were carried out using JPK Nanowizard 3 AFM. Cantilever having gold reflective coating on detector side and resonant frequency of 280 kHz was used for surface structure measurements. Piezo response force microscopy (PFM) measurements were performed using Bruker Dimension Icon AFM-Raman system. Pt/Ir coated conducting cantilever with resonant frequency of 75 kHz was used for PFM measurement. PE hysteresis loop measurements were performed using Trek model 609B, Radiant technologies.inc.

3. Results and discussion

3.1. X-ray analysis

Detailed structural characteristics were examined by X-ray characterization of the electric field (EF) treated films. X-ray diffraction measurements carried out on samples EF treated at 0 V/cm, 5×10^2 V/cm, 1.1×10^3 V/cm, 1.5×10^3 V/cm and 2.1×10^3 V/cm, shown in Fig. 1 reveals a systematic trend.

Lower EF results in a combination of α , β and γ phases coexisting in the film. Major peaks present in the XRD spectrum are 18.0°, 18.7° and 19.8°. Presence of peaks at 18.0°, 18.7° indicate paraelectric α -phase and γ phase coexisting with β phase at lower EF [31]. Intermediate EF, 1.5×10^3 V/cm results in maximum β -phase character, with sharp peak at ~20° and highest crystallinity (Table T2, Supporting Information) as shown in the X-ray diffraction pattern. This angle of 20° is attributed to the β -phase of PVDF-TrFE [30]. Higher β -phase contribution is evident from the Polarization-Electric field curve (PE) as shown in the supporting information Fig. S5 and from the Vertical Piezo response force (VPFM) microscopy images as given in supporting information Fig. S10. The intensity maxima and Full width half maxima (FWHM) of this β -phase feature is a function of EF. A clear and monotonic increase in the intensity accompanied by a decrease in FWHM with EF reveals an increase in order and crystallinity (Table T2, Supporting Information).

3.2. Microstructure and Piezo force response characterization

High resolution AFM imaging of the dielectric layer also reveals a formation of sizable crystalline regions with EF treatment (Fig. 2). This feature of well-defined regions increases with EF up to a threshold electric field (EF_{th}) magnitude. Beyond, this EF_{th} , the domain sizes reduces with larger presence of domain boundaries. AFM topography and phase studies reveal the evolution of PVDF-

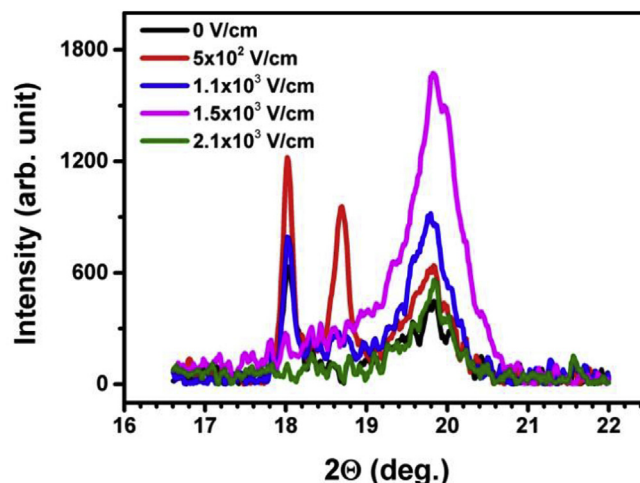


Fig. 1. X-ray spectrum of PVDF-TrFE film grown under various EF.

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