Organic Electronics 42 (2017) 316–321

Contents lists available at ScienceDirect

Organic Electronics

journal homepage: www.elsevier.com/locate/orgel

Surface-induced orientation of pentacene molecules and transport anisotropy on nanogroove SiO_2 dielectric layer by simple scratched method: The study of surface roughness and molecular alignment on the mobility of organic thin film transistors

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ARTICLE INFO

Article history:
Received 1 September 2016
Received in revised form
6 December 2016
Accepted 20 December 2016
Available online 21 December 2016

Keywords:
Nano-groove
Pentacene
Molecular anisotropy
Surface roughness
OTFTs

ABSTRACT

We obtained preferential in-plane molecular orientation and charge-transport anisotropy in pentacene thin-film transistors (TFTs) on conventional SiO_2/Si substrates. The nanoscale SiO_2 grooves with depths of 1–3 nm were prepared by a simple scratching process with diamond powder to create a new type of alignment template for inducing the aligned growth of pentacene with in-plane anisotropy. Results of atomic force microscopy and grazing-incidence X-ray diffraction showed that the nanogrooved SiO_2 structure could control the alignment and growth mode of pentacene, and it remarkably decreased the grain size of the pentacene crystals. The charge-carrier mobility along the parallel axis of the nanogrooved structure (0.392 ± 0.039 $cm^2/(V \cdot s)$) was more than four-fold higher than that perpendicular to the alignment (0.104 ± 0.048 $cm^2/(V \cdot s)$). In addition, we investigated the effect of nanogrooved SiO_2's surface roughness on the electrical properties of the pentacene TFT and found out that the surface roughness of SiO_2 dielectric layer was more crucial factor on the device performance compared to the preferential alignment of the pentacene molecule.

1. Introduction

Organic thin-film transistors (OTFTs) have received significant attention over the past decade for their potential to enable fabrication of low-cost, printable, flexible electronic applications [1–3]. Significant progress has been made in the performance of OTFTs based on small molecules with mobility above 10 $cm^2/(V \cdot s)$ [4,5]. Many studies have focused on improving the performance of small-molecule organic semiconductor (OSC)-based TFTs by optimizing deposition conditions such as the deposition rate [6], substrate temperature [7], roughness [8], and surface treatment [9]. in order to enhancement of crystallinity of small-molecule OSCs. In addition to the growth conditions, the carrier mobility in OTFTs strongly depends on the degree of π-orbital overlap between adjacent molecules [10]. Although some groups have reported a random polymer exhibiting low crystallinity has superior field-effect mobility compared to a highly crystalline conjugated polymer [11], the one of most effective way to increase the carrier mobility is to grow single crystal of organic molecules with an appropriately preferred orientation relative to the source and drain electrodes. This means that the optimal direction of π-orbital overlap should be parallel to the charge-transport direction. In previous works, the preferential alignment of OSC molecules (including pentacene) produced by an orientationally ordered insulator of an extra alignment layer on an insulator was found to enhance the mobility of the resulting OTFT [12,13]. Several methods such as friction-transfer [14], rubbing [15,16], photoalignment [17,18], and nano-patterning [19,20] have been developed to fabricate the alignment layer.

Recently, Heeger's group reported the use of nanogrooved

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http://dx.doi.org/10.1016/j.orgel.2016.12.036
1566-1199/

substrates to obtain chain alignment and the associated anisotropy, with resulting mobilities of 50 $cm^2/(V \cdot s)$ for regioregular polymeric OSCs [21–25]. The aligned polymer thin films exhibited strong anisotropy, showing more than a 10-fold increase in mobility for transport along the direction of alignment compared to that perpendicular to the alignment. This concept of directed self-assembly of semiconducting polymers using nanogrooved substrates is also promising for achieving high mobility in solution-processed flexible OTFTs.

In general, when compared to polymer-based OSCs, small-molecule OSCs are easily affected by their surface morphology or roughness owing to their high crystallinity and small grain size, which is comparable to the channel width of devices [19]. To our knowledge, however, there have been few studies on small-molecule OSCs on nanogrooved SiO_2/Si substrates that are fabricated by easy and cheap processes on large areas. And the effect of roughness of nanogrooved surface on the electrical properties of small-molecule OTFTs is not studied yet.

Here, we report our investigation on the molecular alignment and crystal growth of small-molecule OSCs on nanogrooved SiO_2 dielectric substrates and their application in OTFTs. The nanoscale SiO_2 grooves with depths of 1–3 nm were prepared by a simple scratching process with diamond powder to create a new type of alignment template for inducing the aligned growth of pentacene with in-plane anisotropy [22,26]. In this work, pentacene was chosen as the small-molecule semiconductor, which is commonly used as an active material for OTFTs because of its high stability in air and because its crystal structure has been extensively studied. The charge-carrier mobility along the parallel axis (preferred direction) of the nanogrooved structure (0.392 ± 0.039 $cm^2/(V \cdot s)$) was more than four-fold higher than that perpendicular to the alignment (0.104 ± 0.048 $cm^2/(V \cdot s)$). In addition, we investigated the effect of the nanogrooved SiO_2's surface roughness on the electrical properties of the pentacene TFTs. However, from the device performance point of view, the device was fabricated on a nanogrooved (or scratched) SiO_2 substrates showed poor device performances compared to the reference device with the non-scratched (or smooth) SiO_2 substrate. Although the nano-grooved substrate have been effective to molecular alignment and enhancement of device performance in case of polymer OSCs [21–25], the increased surface roughness induced from nano-groove structure negatively affect the performance of small-molecule OSCs.

2. Experimental section

2.1. Preparation of the nanogrooved SiO_2/Si substrates

The scratching was processed by a typical polishing machine (TegraPol 25, Struers). The polishing plate was covered with a cloth having an attachable 25.4-cm (10-in) magnetic fastening plate. Before polishing, the top surface of cloth was first soaked in a sufficient amount of water, and aqueous polycrystalline diamond (diameter = 1, 3, and 6 μm) suspension (90-32015, Allied High Tech) was sprayed onto the wet cloth. A 2 cm × 2 cm SiO_2/Si substrate was flipped upside down and gently pressed onto the machine while the plate is spinning at 150 rpm, 10 cm away from the rotational axis. After a few seconds of polishing, the scratched substrate was cleaned in standard cleaning process with acetone, isopropyl alcohol (IPA), and deionized (DI) water baths for 10 min each with ultrasonication. Since we used the relatively small sample (2 cm × 2 cm), we could generate linear scratches over the entire substrate. It is noteworthy that scratches were invisible to the naked eye and even under an optical microscope because they were a few nano-sized grooves.

2.2. Microstructural characterization

Atomic force microscopy (AFM; Multimode-8, Bruker) was used in height mode to examine the morphology of the deposited pentacene thin films. Two-dimensional grazing-incidence X-ray diffraction (2D-GIXD) measurements were performed by using the synchrotron source of the 9A beamline at the Pohang Accelerator Laboratory (PAL) in Korea. Samples with dimensions of 10 mm × 10 mm were prepared and guided into the path of a focused X-ray beam with energy of 11.146 keV and size of 70 μm (vertical) by 300 μm (horizontal). The sample-to-detector distance (SDD) was 234.6 mm, and the diffraction patterns were mostly acquired for 1–10 s with a two-dimensional charge-coupled device (2D CCD) detector.

2.3. Device fabrication and characterization

To assess the electrical performance of the pentacene TFTs, bottom-gate, top-contact TFTs were fabricated on a 100-nm thick (non-patterned or nanogrooved) SiO_2/Si substrate. A 60-nm-thick layer of pentacene (Sigma-Aldrich) was deposited on top of the SiO_2 gate dielectric layer through a shadow mask by thermal evaporation at a pressure 1×10^{-6} Torr. The evaporation rate of the pentacene was 1 Å/s, and the substrate temperature was 90 °C. Top-contact 50-nm-thick Au source and drain electrodes were fabricated on the pentacene films, either parallel or perpendicular to the long axis of the nanogrooves. The channel length (L) and a width (W) were 50 and 1000 μm, respectively. The transfer characteristics (I_{ds} vs. V_{gs}) of the TFT devices were measured with a semiconductor parameter analyser (E5272, Agilent). All electrical measurements were performed under dark ambient conditions.

3. Results and discussion

To determine the effects of the nanoscale grooved structure on the crystal growth of pentacene with terrace-like grains on the SiO_2 dielectric layer and on the electrical properties of the resulting crystals in an OTFT, surface grooves were introduced on p-doped silicon wafers with a 100-nm-thick SiO_2 gate dielectric insulating layer by scratching the surface using polishing diamond powders with diameters of 1, 3, and 6 μm. In this study, we adopted the floating-polishing method to generate the parallel lines of scratches, as described in our previous work [26]. Fig. 1 shows the schematics and AFM images of the nanogrooved structure on SiO_2 prepared by the scratching technique. The tips of the micometer-sized diamond particles made contact with the substrate only during scratching, yielding nanoscale grooves, as shown in Fig. 1a and b. However, we found that as the diamond particle size increased, the density of grooves tended to decrease, while the depth of the grooves slightly increased, as shown in Fig. S1 in Supporting Information. As the size of particles increased, the probability of contact between the diamond particles and the SiO_2 substrate decreased as shown in schematic draw in Fig. S2. Thus, the frequency of nanogrooves generated when using large-sized diamond particles is smaller. Using larger size diamond particles to create higher density of nanogrooves, the SiO_2 surface is severely damaged or very deep nanogrooves of more than 10 nm are formed. It was clearly observed here that finer control over the groove depth could be achieved when smaller particles were used to polish the substrate. In this study, mostly nanogrooved SiO_2/Si substrates scratched by 1-μm-diameter diamond particles were used for other procedures such as characterization of nanostructure and electrical properties (discussed below).

After the scratching process, the water contact angle of the SiO_2 gate insulator remained at ~40°, as shown in Fig. 1c. It means that