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A new systolic multiprocessor architecture for real-time soft tomography algorithms

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ABSTRACT

In this paper, a new systolic multiprocessor architecture for soft tomography algorithms that explores the intrinsic parallelisms and hardware resources which are available in recent Field Programmable Gate Arrays architectures is presented. The soft tomography algorithms such as Electrical Capacitance Tomography (ECT), Magnetic Inductance Tomography (MIT), and Electrical Impedance Tomography (EIT), while they use different sensors and data acquisition modules, they feature common computation requirements which consist of intensive matrix multiplications and fast/frequent memory accesses. Using the variable bit-width and fixed-point multipliers array available in the DSP blocks, which cooperatively perform the partial matrix product with associated Arithmetic and Logic Units (ALU), and distributed memory available in Stratix V FPGA, a dedicated scalable architecture is suggested to host the Landweber algorithm. The experimental results indicate that 16,949 frames of (32×32 pixels) can be reconstructed in one second if each element of the matrix is attributed to 18 bits and using a clock frequency of 400 MHz. This is more than enough in most process imaging applications. In addition, the accuracy of the image reconstruction using 18 bits/operand is found to be acceptable since it exceeds 86%. More accuracy can be achieved up to 99% if 36 bits/operand are used which leads to an image reconstruction throughput of 1272 frames /s (for image size 32×32).

1. Introduction

Soft Tomography algorithms (e.g. Magnetic Induction Tomography, MIT, Electrical Capacitance Tomography, ECT, and Electrical Impedance Tomography, EIT) are gaining increasing interest in various applications such as process and biomedical imaging as compared to their hard-tomography algorithms counterparts (e.g. X-ray tomography) due to the fact that they are less hazardous and much faster [1,9]. However, these algorithms still require intensive matrix multiplications and frequent memory access making them still not suitable for real-time applications where a throughput of at least tens of frames per second is required. In spite of the progress in the integration scale and architectures of modern microprocessors and Digital Signal Processors (DSP) (i.e. VLIW or superscalar architecture), they still share the same concept than older processors, where a static set of instructions is run in a static architecture. Nevertheless, they have the advantages to perform strong control-oriented applications and can be easily reprogrammed [2]. Field Programmable Gate arrays have the advantages to feature dense fine parallelism where hundreds of instructions can be executed at once, in addition to be reprogrammable, which is suitable for most tomography algorithms. Hence, in [3], a comparison study on the DSP versus FPGA-based architectures

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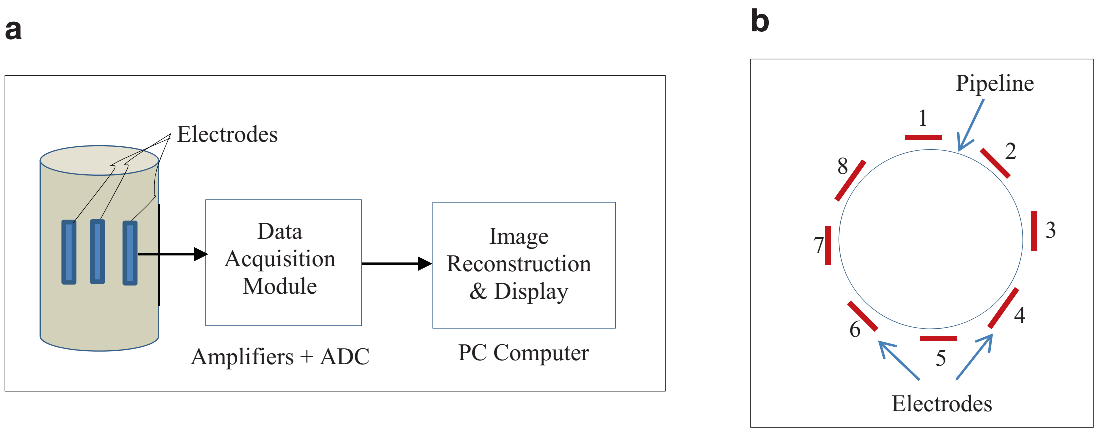

Fig. 1. An Overview of an ECT system: (a) The overall hardware system (b) front view of the ECT sensor.

was done with regard to the Linear Back Projection (LBP) algorithm. The corresponding results revealed that the FPGA-based architecture could provide a speed-up of about 18 and 4.6 over a single DSP processor and four-DSP processors-based architectures respectively. The two architectures used the multiply and accumulate (MAC) units to perform sequentially all the matrix multiplication of the LBP algorithm. Nevertheless, the architecture presented in this paper is different in a way that the matrix multiplication hardware explores the fine parallelism of the actual FPGA circuits and uses a higher number of regularly arranged processing elements. Furthermore, and contrary to their work, this paper also addresses a not-less important issue of assessing the effect of fixed point quantization on the image quality.

In this paper, we present a new VLSI architecture of tomography algorithm using FPGA technology. The architecture is flexible enough to host different image sizes and explores some of the new features of recent FPGA devices (i.e. Stratix V-5SGTC7) such as the DSP blocks and the Block RAM (BRAM). To the best of the authors' knowledge, this is the first embedded system which explores the intrinsic parallelism which is available in modern FPGA for soft tomography algorithms and can be suitable for ECT, MIT, and/or EIT algorithms. The FPGA selected in this study is Stratix V FPGA which is the most recent FPGA IC available in the market. It features several parameters which are suitable for real-time tomography algorithms such as high density (1 million) of Logic Elements (LE) and high speed transceivers for fast sensor interfacing (around 14 Gbps). experimental results indicate that 16,949 frames of (32 × 32 pixels) can be reconstructed in one second if each element of the matrix is attributed to 18 bits and using a clock frequency of 400 MHz. This is more than enough in most process imaging applications. In addition, the accuracy of the image reconstruction using 18 bits/operand is found to be acceptable since it exceeds 86%. More accuracy can be achieved up to 99% if 36 bits/operand are used which leads to an image reconstruction throughput of 1272 frames/s (for image size 32 × 32).

2. System overview

Fig. 1 shows a typical soft tomography system such as ECT system [1,4]. It mainly consists of a set of electrodes which surround the process under investigation, a multiplexing unit to provide different combinations of capacitance channels, and a computing device (usually a general purpose computer) to run the tomography algorithms. Besides the electrodes, all the other hardware modules are similar to those found in other soft tomography systems. Hence, in this paper the ECT system is used as an example which can be extended to other modalities as well.

2.1. Theoretical background

In ECT, the multi-electrode model can be characterized by the following Poisson's equation:

$$\nabla(\varepsilon_0 \varepsilon(x,y) \nabla\phi(x,y)) = 0 \tag{1}$$

Where ∇ is the gradient permittivity distribution function, $\varepsilon(x,y)$ the permittivity distribution function, $\phi(x,y)$ the electric potential distribution function, and ε_0 the vacuum permittivity, which is equal to 8.85×10^{-12} F/m. The capacitance values of individual pairs can be obtained using the following equation [4]:

$$C_{i,j} = -\left(\oint_{\Gamma} \varepsilon(x,y).\nabla\phi(x,y)d\Gamma\right) \Big/ (\phi_i - \phi_j) \tag{2}$$

where $(\phi_i - \phi_j)$ denotes the electric potential difference between the excitation electrode, i, and the detection electrode, j; and Γ denotes a closed area surrounding the electrodes i and j. The linearized model of the forward problem of ECT system,