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Transparent field-effect transistors based on AlN-gate dielectric and IGZO-channel semiconductor

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ABSTRACT

The degradation of thin-film transistors (TFTs) caused by the self-heating effect constitutes a problem to be solved for the next generation of displays. Aluminum nitride (AlN) is a viable alternative for gate dielectric of TFTs due to its good thermal conductivity, matching coefficient of thermal expansion to indium–gallium–zinc-oxide, and excellent stability at high temperatures. Here, AlN thin films of different thicknesses were fabricated by a low temperature reactive radio-frequency magnetron sputtering process, using a low cost, metallic Al target. Their electrical properties have been thoroughly assessed. Furthermore, the 200 nm and 500 nm thick AlN layers have been integrated as gate-dielectric in transparent TFTs with indium–gallium–zinc-oxide as channel semiconductor. Our study emphasizes the potential of AlN thin films for transparent electronics, whilst the functionality of the fabricated field-effect transistors is explored and discussed.

1. Introduction

The fabrication of suitable dielectric thin films at low temperatures represents a mandatory step toward efficient, transparent and low cost flexible electronics. The most important criteria a dielectric material must fulfill are: a band gap higher than the semiconductor (>5 eV is desirable) and a favorable conduction or valence band offset (for n- and p-type semiconductors, respectively) in order to minimize the gate leakage current. The good quality of the dielectric-semiconductor interface is also very important because the transistor performance can be very poor if the gate insulator leads to excessive interface states.

Nowadays the most commonly used dielectric in thin film transistors (TFT) is SiO_2 [1–3]. However, because of its poor thermal conductivity [4], the application of SiO_2 as insulating layer in high-power, high-temperature logic devices is limited by the self-heating effect [5]. Even in applications where power and temperature are more conservative, as in displays, self-heating can also be significantly affected by the dielectric layer, as heat dissipation to ambient in TFTs is primarily made through the gate contact via the gate insulator [6]. The overheating of the devices causes the degradation of the operations and the reduction of functionality and lifetime. Therefore, the development of new insulating materials with good thermal conductivity and high dielectric constants is mandatory, and research on this topic experienced a unique effervescence in recent years [7–18].

The aluminum nitride (AlN) dielectric can overcome the above mentioned issues. AlN is an III–V semiconductor with hexagonal wurtzite lattice which exhibits a wide energy band gap of approximately 6.2 eV [19,20].

AlN exhibits a high thermal conductivity of $\sim 17\,W\,m^{-1}\,K^{-1}$ in thin film (150 nm) form [21], more than ten times higher than SiO_2 ($\sim 1.3\,W\,m^{-1}\,K^{-1}$) of similar film thickness, a low thermal expansion coefficient ($\sim 5.3 \cdot 10^{-6}\,K^{-1}$), high intrinsic resistance ($>10^{13}\,\Omega\,cm$), good dielectric strength ($3 \cdot 10^{6}\,V\,cm^{-1}$, this work) [22,23] and good stability at high temperatures [24]. Therefore, the use of AlN as gate-dielectric layer should reduce the influence of the self-heating effect observed in TFTs.

Moreover, AlN is a low cost material which can be obtained at low temperature (<50 °C) at a relatively high deposition rate ($16\,nm\,min^{-1}$) by reactive deposition using a simple aluminum target [25–27]. The high deposition rate is a major advantage for the device fabrication, as thick AlN layers can be deposited in a short time, preventing thus the overheating caused by the plasma radiation. Also, the high deposition rate imprints certain economical advantages (e.g. production time-cost efficiency). In the proposed technological algorithm, the AlN deposition temperature never exceeds 50 °C, which is significantly below the photoresist

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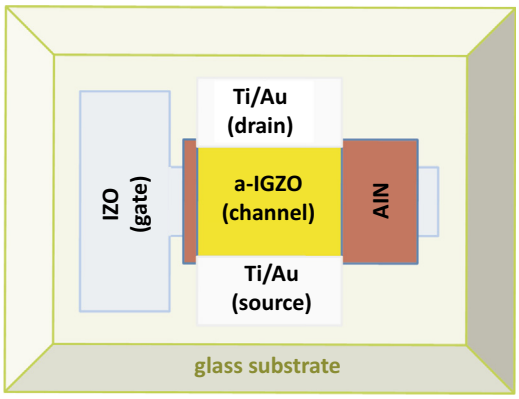

Fig. 1. Schematic diagram depicting the architecture of the IGZO-AlN TFT devices.

degradation temperature (~130 °C). This enables one to use simpler patterning routes such as lift-off, where selectivity is not an issue, as opposed to the more traditional chemical etching processes.

Due to its piezoelectric properties, AlN was widely used for the fabrication of high frequency electro-acoustic devices, such as resonators and sensors, based on bulk or surface acoustic wave filters (BAW or SAW) [28–30].

Somehow in contradiction with its promising properties, AlN has been very rarely used in thin-film transistors (TFT) manufacturing [31–34], but never as gate insulator in fully transparent transistors or in combination with indium–galium–zinc-oxide (IGZO), which is, nowadays, the most promising candidate able to substitute the conventional amorphous Si:H in active matrix liquid crystal displays and organic light emitting diodes [35–37]. Furthermore, due to its matching coefficient of thermal expansion to IGZO ($5.3 \cdot 10^{-6}$ K^{-1} for AlN vs. $5.23 \cdot 10^{-6}$ K^{-1} for IGZO [38,39]), AlN could become pivotal in the development of high-quality transparent TFTs.

In this study the electrical properties of AlN thin layers are investigated in the view of developing reliable gate dielectrics for transparent TFTs with IGZO as semiconductor. Devices were fabricated using optimized gate dielectric AlN layers. Their Current–Voltage (*I–V*) transfer and output characteristics, as well as their electrical stability undergoing gate bias stress of +20 V are explored and discussed.

2. Experimental

2.1. Device fabrication

AlN thin films with thicknesses of 50, 100, 150, 200 and 500 nm were obtained at low temperature (~50 °C) by reactive radio-frequency magnetron sputtering (RF-MS), using a high purity (99.9995%) Al target (Angstrom Sciences, Inc.). The deposition procedure together with the optical properties of the films are described in detail elsewhere [27].

Further, based on structural and electric assessments, only the 200 and 500 nm thick AlN layer were integrated as gate dielectric into TFTs (Fig. 1). The two sets of staggered bottom-gate transistors were fabricated on glass substrates using photolithography and lift-off process, and consisted of 17 individual devices. The amorphous IGZO (a-IGZO) n-type semiconductor layers, having a thickness of 30 ± 3 nm, were prepared at room temperature by reactive RF-MS, at a constant total pressure of 0.3 Pa, using a working atmosphere of argon and oxygen (oxygen partial pressure of 0.02 Pa). The indium zinc oxide (IZO) transparent gate electrodes (n-type) were deposited by RF-MS following the procedure described in detail elsewhere [40,41]. The source/drain contacts consist of 6 nm thick Ti and 65 nm thick Au bi-layers which were evaporated by e-beam.

We note that the AlN layers were deposited in typical laboratory conditions (as the sputtering system dedicated for the synthesis of this material is not located in a clean room), whilst the rest of the device fabrication steps were performed under clean room environment.

After fabrication, the transistors were annealed in air, for 90 min, at 200 °C, on a hot plate.

2.2. Characterization methods

(i) The crystalline status of the deposited films was investigated with a Bruker D8 Advance X-ray diffractometer, with Cu-$K_{\alpha 1}$ ($\lambda = 1.5418$ Å) radiation, using a high efficiency linear detector of Lynx Eye type. The films were scanned in the angular range $2\theta = 15 - 80°$ with a step size of 0.04° and 6 s acquisition time per step.

(ii) The surface morphology of films was analyzed by Atomic Force Microscopy in non-contact mode using an NT-MDT NTEGRA Probe NanoLaboratory system (NT-MDT NSG01 cantilever with tip radius of 10 nm).

(iii) The breakdown voltage tests were performed, on metal-insulator-metal (MIM) structures, using a Keithley 2400 source-meter. The Capacitance–Voltage (*C–V*) and Capacitance–frequency (*C–f*) measurements for AlN layers were recorded using Keithley 4200-SCS systems at room temperature, in vacuum, in dark conditions, while the Capacitance–Voltage (*C–V*) and Conductance–Voltage (*G–V*) measurements were made at 300 K using Hioki 3532-50 bridge. An A.C. voltage of 0.1 V, with a delay of 0.5 s was used. The TFT characteristics and the positive gate bias stress tests were carried out at ambient pressure and in the dark using an Agilent 4155C semiconductor analyzer. The stress/recovery periods were shortly interrupted to assess the transfer characteristics on the TFTs.

The subthreshold swing (S) was considered as the minimum value of $(dlog(I_{DS})/dV_{GS})^{-1}$ where I_{DS} and V_{GS} are drain-source current and voltage, respectively. The field effect mobility was extracted from the linear operation regime using the following formula (1):

$$\mu = \frac{L \cdot g_m}{W \cdot C_i \cdot V_{DS}} \quad (1)$$

where $L = 20$ μm is the channel length, g_m is the transconductance, $W = 10$ μm is the channel width and C_i is the gate capacitance per unit area.

3. Results and discussion

The XRD patterns recorded in symmetric geometry for the AlN films with different thicknesses (50, 100, 150, 200 and 500 nm) are displayed in Fig. 2. All layers elicited a pronounced *c*-axis texturing, their crystalline quality being improved with the increase of film thickness (Fig. 2b), evolving from a rather disordered structure (at ~50 nm) to a well-developed highly crystalline film (at ~500 nm). Furthermore, the decrease of the full width at half maximum (FWHM) of the 002 diffraction maximum offers consensual proofs that the average crystalline coherence length enhances in gradual manner (Fig. 2b). This was to be expected, since AlN films, deposited by reactive RF-MS at low temperature on Si wafers with native oxide, are also known to exhibit a progressive ordering and a better alignment along *c*-axis toward the film surface with the increase of film thickness [27].

The breakdown voltage tests were performed for the 100, 150, 200 and 500 nm thick AlN films. As can be observed in Fig. 3, the breakdown field is increasing with the film thickness, being higher