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Ultrathin SiO_2 layer formed by the nitric acid oxidation of Si (NAOS) method to improve the thermal-SiO_2/Si interface for crystalline Si solar cells

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ABSTRACT

A combination of the nitric acid oxidation of Si (NAOS) method and post-thermal oxidation is found to efficiently passivate the SiO_2/n-Si(100) interface. Thermal oxidation at 925 °C and annealing at 450 °C in pure hydrogen atmosphere increases the minority carrier lifetime by three orders of magnitude, and it is attributed to elimination of Si dangling bond interface states. Fabrication of an ultrathin, i.e., 1.1 nm, NAOS SiO_2 layer before thermal oxidation and H_2 annealing further increases the minority carrier lifetime by 30% from 8.6 to 11.1 ms, and decreased the interface state density by 10% from 6.9×10^9 to $6.3 \times 10^9 eV^{-1}\ cm^{-2}$. After thermal oxidation at 800 °C, the SiO_2 layer on the NAOS-SiO_2/Si(100) structure is 2.26 nm thick, i.e., 0.24 nm thicker than that on the Si(100) surface, while after thermal oxidation at 925 °C, it is 4.2 nm thick, i.e., 0.4 nm thinner than that on Si(100). The chemical stability results from the higher atomic density of a NAOS SiO_2 layer than that of a thermal oxide layer as reported in Ref. [28] (Asuha et al., 2002). Higher minority carrier lifetime in the presence of the NAOS layer indicates that the NAOS-SiO_2/Si interface with a low interface state density is preserved after thermal oxidation, which supports out-diffusion oxidation mechanism, by which a thermal oxide layer is formed on the NAOS SiO_2 layer.

1. Introduction

Passivation of a Si interface has been an important process to increase the energy conversion efficiency of crystalline Si solar cells [1–3]. Interface states work as recombination centers of photo-generated electron-hole pairs. The Si interface states decrease the internal quantum efficiency (IQE) below 400 nm of the incident light by which electron-hole pairs are generated near the Si interfaces. The front Si surfaces in commercial crystalline Si solar cells are usually passivated by deposition of a silicon nitride (SiN) layer which contains high concentration of hydrogen. Thermal oxidation above 900 °C is a candidate for a rear Si surface passivation method, e.g., in passivated emitter and rear locally diffused cells (PERL), and passivated emitter and rear cells (PERC) [4]. These methods passivate Si surfaces by elimination of Si dangling bond defect states, e.g., by the formation of Si-H bonds resulting from the reaction with hydrogen. Another passivation method utilizes charges induced at Si/insulator layer interfaces (field-effect passivation) [5–8]. Positive charges (e.g., Si/SiN interfaces [5,6]) and negative charges (e.g., Si/Al_2O_3 interfaces [7,8]) repulse holes and electrons, respectively, preventing these charges to approach the interfaces, thus, avoiding electron-hole recombination at the interfaces.

We have developed a low temperature fabrication method of Si/SiO_2 structures which simply involves immersion of Si in high concentration nitric acid (HNO_3) for a few minutes, i.e., nitric acid oxidation of Si methods (NAOS) [9–11]. The NAOS method can provide an ultrathin (i.e., 0.7–1.4 nm) SiO_2 layer with excellent electrical properties. In the case of a gate dielectric layer in thin film transistors (TFTs), its thickness can drastically be decreased to e.g., 10 nm by insertion of a NAOS SiO_2 layer between the Si substrate and a plasma-enhanced chemical vapor deposition (CVD) SiO_2 layer because the NAOS SiO_2 layer acts as a leakage current blocking layer [9–14].

By use of the NAOS method in crystalline Si solar cells, the energy conversion efficiencies of both n-type (bifacial Passivated Emitter Real Totally-diffused, PERT) and p-type (Al-BSF) mono-Si solar cells

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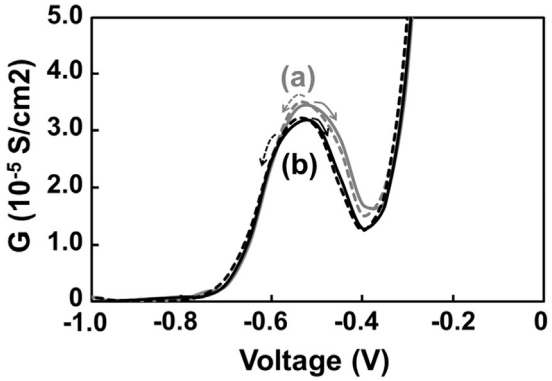

Fig. 1. G-V curves at 10 kHz for the <Al/SiO_2/n-Si(100)> structure after thermal oxidation at 925 °C: a) without the NAOS treatment, b) with the NAOS treatment performed before thermal oxidation. The solid and dotted lines indicate G-V curves measured during forward and reverse sweeps, respectively. The arrows indicate the voltage sweep direction.

have increased from 17.2 to 18.9% and from 16.6 to 17.5%, respectively, because of low interface state density characteristics [1,2]. Furthermore, post-thermal oxidation of a NAOS layer on a flat p-Si(111) surface at 800 °C has been found to increase the minority carrier lifetime from 12 μs to 45 μs in our laboratory. Therefore, it is expected that the combination of the NAOS method and thermal oxidation greatly decreases the interface state density, leading to a higher energy conversion efficiency of Si solar cells.

In this study, we have demonstrated that the NAOS method plus thermal oxidation can effectively passivate Si surfaces.

2. Experiments

A phosphorus-doped n-type mirror-polished CZ-Si(100) wafer with resistivity of 8–12 Ωcm was used for the substrate. An ultrathin NAOS SiO_2 layer was formed by immersion of the Si wafer in a 68 wt% HNO_3 aqueous solution at 80 °C for 10 min. The thickness of a NAOS SiO_2 layer was estimated to be 1.1 nm by an X-ray photoelectron spectroscopy (XPS) measurement. Thermal oxidation was conducted at temperatures between 700 and 1000 °C for 10 min in pure dry-oxygen atmosphere. Subsequent annealing was carried out at 450 °C in 100% hydrogen atmosphere for 30 min.

Minority carrier lifetime measurements of a <NAOS-SiO_2/Si/NAOS-SiO_2> symmetric structure were performed by use of the microwave photo-conductivity decay (μ-PCD) method using a Kobelco LT-1512 apparatus with 904 nm wavelength incident light. Conductance-voltage (G-V) measurements of a <Al/SiO_2/Si> metal-insulator-semiconductor (MOS) structure were performed by use of an HP 4192A LF impedance analyzer. Oxide thickness was measured by a spectroscopic ellipsometry using a SOPRA GES-5 ellipsometer. XPS measurements were carried out using a KRATOS AXIS-165x spectrometer with a monochromatic Al Kα radiation source.

3. Results and discussion

Fig. 1 shows the conductance-voltage (G-V) curves for the <Al/SiO_2/n-Si(100)> MOS structure with and without the NAOS treatment after thermal oxidation at 925 °C in dry oxygen and annealing at 450 °C in 100% H_2 atmosphere. The HNO_3 treatment decreased the peak height, indicating a decrease in the interface state density [15].

Fig. 2 shows the interface state density calculated from the G-V curves for the thermal oxidation temperatures at 800–1000 °C. For the estimation, the averages of the G-V curves measured during forward and reverse sweeps were adopted after subtraction of the

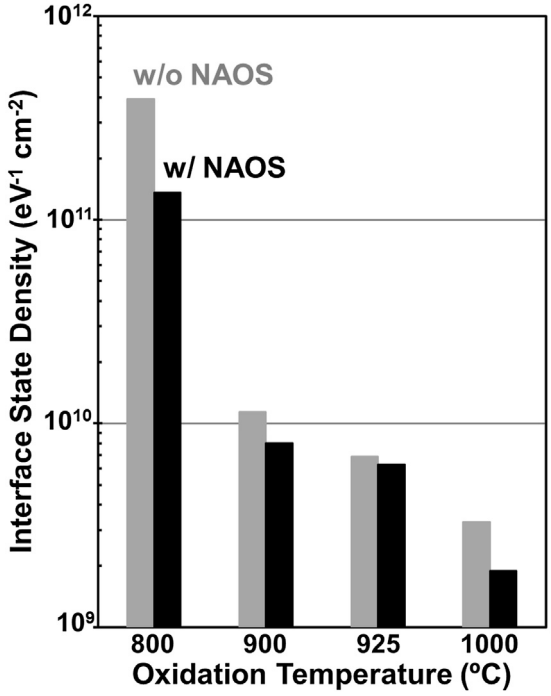

Fig. 2. Interface state density for the <Al/SiO_2/n-Si(100)> MOS structure with and without the NAOS treatment vs. the thermal oxidation temperature.

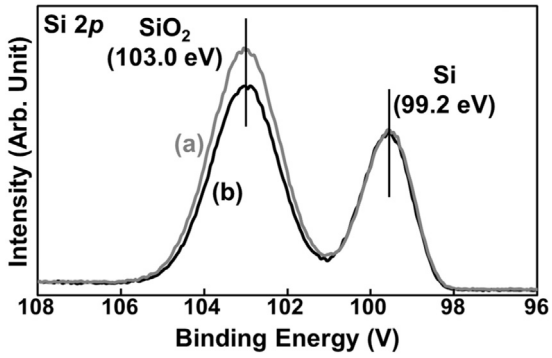

Fig. 3. XPS spectra of the SiO_2/n-Si(100) structure after thermal oxidation at 925 °C: a) without the NAOS treatment; b) with the NAOS treatment performed before thermal oxidation.

background. The narrow hysteresis and the background of the G-V curves are most probably due to slow states [16] and a leakage current [17], respectively. The interface state density, D_{is}, can be calculated using the following equation [15]:

$$D_{is} = \frac{2}{eA}\left(\frac{G}{\omega}\right), \quad (1)$$

where A is the electrode area, and G is the maximum conductance at the angular frequency of ω. In Fig. 2, D_{is} calculated from the conductance at 10 kHz is adopted because the conductance peak in the frequency range between 10 and 100 kHz is attributable to interface states at the SiO_2/Si interface [18,19]. The interface state density drastically decreased with the thermal oxidation temperature, in good agreement with the previous literatures [20,21]. With the NAOS treatment performed before thermal oxidation, the interface state density was lower by 10–60% than those without it.

Fig. 3 shows the XPS spectra in the Si 2*p* region for the SiO_2/Si(100) structure with (spectrum b) and without (spectrum a) the NAOS treatment performed before thermal oxidation at 925 °C. The XPS spectra were normalized by the peak intensities for the

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