G Model
APSUSC-33024; No. of Pages 6
ARTICLE IN PRESS
Applied Surface Science xxx (2016) xxx–xxx

Contents lists available at ScienceDirect
Applied Surface Science
journal homepage: www.elsevier.com/locate/apsusc

Analysis of low temperature output parameters for investigation of silicon heterojunction solar cells

Miroslav Mikolášek*, Juraj Racko, Ladislav Harmatha

Slovak University of Technology, Faculty of Electrical Engineering and Information Technology, Institute of Electronics and Photonics, Ilkovičova 3, 812 19 Bratislava, Slovakia

ARTICLE INFO

Article history:
Received 29 January 2016
Received in revised form 31 March 2016
Accepted 4 April 2016
Available online xxx

Keywords:
Solar cell
Amorphous silicon
Heterojunction
Schottky barrier
TCO/a-Si:H
ASA simulation
Low temperature
Open circuit voltage

ABSTRACT

This paper presents an ASA simulation analysis of temperature dependent output parameters of the silicon heterojunction (SHJ) solar cell. The analysis has shown that low temperature behaviors of the open circuit voltage and fill factor are strongly connected with the presence of barriers for collection of photogenerated carriers in the SHJ structure. Previous experimentally observed saturation of the open circuit voltage at low temperature was attributed to the presence of a parasitic Schottky barrier at the transparent conductive oxide/amorphous emitter contact. A comprehensive simulation study is provided to describe the mechanism of such saturation and to define the conditions under which the saturation of the open circuit voltage can be used as relevant identification of the parasitic Schottky barrier in SHJ structures with both n-type and p-type amorphous emitters. In addition, the presented study provides the first guideline on the possible utilization of SHJ in low temperature applications such as space applications.
© 2016 Elsevier B.V. All rights reserved.

1. Introduction

Silicon heterojunction (SHJ) solar cell is a promising technology with the perspective to combine the low temperature deposition process of amorphous silicon and the high efficiency of crystalline silicon solar cells [1,2]. Recently, the record efficiency of 25.6% [3] was achieved on SHJ, which makes this technology the most efficient among the silicon based solar cells. The superiority of SHJ compared to standard crystalline solar cell stems from the heterojunction formed between (a-Si:H) and crystalline silicon (c-Si) which, due to the band discontinuity, provides a high build-in voltage and thus a high open-circuit voltage (V_{oc}). Utilization of a-Si:H as an emitter in the SHJ solar cell is connected with a number of challenging requests regarding the quality of this layer and its interfaces. On the one hand, the defect states and band alignment at the a-Si:H/c-Si interface determine the carrier inversion at the interface and thus recombination and collection of light generated carriers [4–6]. On the other hand, low specific conductivity of a-Si:H requires to use transparent conductive oxides (TCO) as a collection electrode. When not properly prepared, the parasitic Schottky barrier can be formed at the TCO/a-Si:H interface [7–9]. Such a Schottky barrier has its origin in the interlayer formed at the TCO/a-Si:H interface or in the material properties of TCO and hinders the collection of photogenerated carriers, which results in deterioration of the overall efficiency. The properties of the a-Si:H [10,11] layer as well as of the a-Si:H/c-Si and a-Si:H/TCO heterojunctions are the most critical factors for achieving high performance of SHJ [1,12]. Strong attention of researchers is focused on the investigation of the a-Si:H/c-Si interface, which resulted into the development of a number of diagnostics techniques for measurement of defect states [13–15] and band offset [16,17]. However, only limited attention is focused on the non-perfect TCO/a-Si:H contact properties in SHJ. The requirement of good ohmic quality of the TCO/a-Si:H interface is very important for low temperature applications. Due to the strong decrease of thermionic emission with decreasing temperature, the effect of the parasitic Schottky barrier becomes more significant for these applications. In the recent experimental study carried out at ZnO/a-Si:H(n)/a-Si:H(i)/c-Si(p)/c-Si(p^+)/Al structure, the V_{oc} saturation was observed at low temperatures, which was attributed to the parasitic Schottky barrier at the TCO/a-Si:H interface [18]. It was suggested that measuring of the solar cell output parameters in dependence on temperature below 300 K can be used as a method for identification of the limiting properties such as the parasitic Schottky barrier at the TCO/a-Si:H interface, which hinder the transport and collection of photogenerated carriers in the

* Corresponding author.
E-mail address: miroslav.mikolasek@stuba.sk (M. Mikolášek).

http://dx.doi.org/10.1016/j.apsusc.2016.04.023
0169-4332/© 2016 Elsevier B.V. All rights reserved.

Please cite this article in press as: M. Mikolášek, et al., Analysis of low temperature output parameters for investigation of silicon heterojunction solar cells, Appl. Surf. Sci. (2016), http://dx.doi.org/10.1016/j.apsusc.2016.04.023

structure. However, physical explanation of V_{oc} saturation at low temperature and its dependence on various properties of a-Si:H and a-Si:H/c-Si interfaces remain still unclear. This paper presents a comprehensive ASA simulation study to obtain a deeper insight into the carrier transport properties through the TCO/a-Si/c-Si emitter stuck of both a-Si:H(n)/c-Si(p), in the text labeled as SHJn, and a-Si:H(p)/c-Si(n), in the text labeled as SHJp structure. The possible utilization of low temperature light current-voltage measurements under illumination is discussed for investigation of SHJ solar cells and for identification of the parasitic Schottky barrier at the TCO/a-Si:H interface. In addition, the results provide the first guideline for utilization of SHJ for space applications, where the operation conditions are deep below 300 K.

2. Simulation set-up

The ASA 5.2 software was used for simulation of temperature dependent solar cell output parameters of SHJ structures. The ASA program is designed for the simulation of devices based on amorphous and crystalline semiconductors. It uses several advanced physical models implied from the spatial disorder in the atomic structure of a-Si:H, which are employed to describe the trapping and generation/recombination processes in the amorphous silicon [19]. The ASA program solves the basic semiconductor equations in one dimension (the Poisson equation and two continuity equations for electrons and holes) and uses the free electron concentration, n, the hole concentration, p, and the electrostatic potential, ψ, as variables.

Two simulation models with layer sequence TCO/a-Si:H(n)/a-Si:H(i)/c-Si(p)/c-Si(p^+)/Al and TCO/a-Si:H(p)/a-Si:H(i)/c-Si(n)/c-Si(n^+)/Al are defined for SHJn and SHJp structures, respectively. For a-Si:H layers, parameters such as the band gap, doping, energy distribution of defect states in the forbidden gap are chosen based on reference [5,20,21] and tuned to fit the measured optoelectronic properties of the deposited a-Si:H layers. Input parameters of the models are listed in Table 1. Default model of c-Si is considered with lifetime of 100 μs. The doping concentration of 1×10^{18} cm^{-3} is set for both Si(p^+) and Si(n^+). Such layers with thickness of 500 nm act as a back surface field (BSF) and are defined by the standard parameters for n and p type c-Si. The defect states at the a-Si:H/c-Si interface are modeled by introduction of 1 nm thick highly defective layer between amorphous and crystalline silicon layers. The defective layer is defined by using the crystalline silicon parameters and with constant distribution of acceptor and donor defects in the forbidden band. The conduction band offset of 150 meV and valence band offset of 450 meV are defined at the a-Si:H/c-Si interfaces for SHJn and SHJp structures, respectively. As an illumination source the power density of 100 mW/cm^2 (AM1.5) is adopted.

3. Results and discussion

3.1. Temperature dependence of FF and V_{oc}

Among the solar cell output parameters, the open circuit voltage, V_{oc} and fill factor, FF are strongly affected by the carrier transport and collection in the structure and thus investigation of such parameters should provide information about the limiting properties for carrier transport in the solar cell. V_{oc} corresponds to the state where the total rate of photogeneration equals the rate of recombination. The temperature dependence of V_{oc} is thus determined by the temperature dependence of the generation–recombination balance [22]. In general, the temperature behavior of V_{oc} can be expressed as [23]

$$V_{OC} = \frac{nkT}{q} \ln\left(\frac{J_{SC}}{J_{Sat}}\right), \quad (1)$$

where J_{Sat} and J_{SC} are saturation current and short circuit current, respectively, q is the elementary charge, T is temperature, k is the Boltzmann constant and n is the diode ideality factor. J_{Sat} is strongly determined by the intrinsic concentration in a semiconductor with a lower concentration of dopants. The exponential decrease of the intrinsic concentration with decreasing T causes an exponential decrease of J_{Sat} and hence results into a linear increase of V_{oc} with temperature.

FF is a very complex parameter related to the transport properties of carriers in the structure. FF as a function of T can be expressed by an empirical equation for silicon based solar cell [24]

$$FF = \frac{V_{OC} - (kT/q)\ln(qV_{OC}/kT + 0.72)}{V_{OC} + kT/q}. \quad (2)$$

Both equations represent only a simple approximation of V_{oc}-T and FF-T behaviors and do not take into account all aspects of defect states, band discontinuities, and material properties of the layers in the structure. Fig. 1 shows V_{oc} and FF measured at the ZnO/a-Si:H(n)/a-Si:H(i)/c-Si(p)/c-Si(p^+)/Al structure as a function of T. The dopant activation energy of a-Si:H(n) in the structure was 0.25 eV [25]. Further details of sample fabrication and measurements are described in [18,25]. While Eqs. (1) and (2) predict an increase of both V_{oc} and FF with a decrease of T, the measured curves exhibit saturation of V_{oc} and decrease of FF at low temperatures. We can assume that the difference between measurements and theory is due to the SHJ properties, which limits the carrier transport in the

Table 1
ASA input parameters used in the simulation.

Parameter	c-Si(p)	c-Si(n)	a-Si:H(i)	a-Si:H(p)	a-Si:H(n)
Layer thickness (μm)	200	200	0.005	0.01	0.01
Band gap (eV)	1.12	1.12	1.75	1.8	1.75
Effective conduction band density (cm^{-3})	2.8×10^{19}	2.8×10^{19}	2×10^{20}	2×10^{20}	2×10^{20}
Effective valence band density (cm^{-3})	1.04×10^{19}	1.04×10^{19}	2×10^{20}	2×10^{20}	2×10^{20}
Electron mobility (cm^2 V^{-1} s^{-1})	1040	1040	20	10	10
Hole mobility (cm^2 V^{-1} s^{-1})	412	412	10	5	5
Acceptor doping con./E_{acc} (cm^{-3}/ eV)	1×10^{15}	0	–	0.45	0
Donor doping con./E_{don} (cm^{-3}/ eV)	0	0.8×10^{15}	–	0	0.25
DOS at CB mobility edge (cm^{-3})	–	–	4×10^{21}	1×10^{22}	7×10^{21}
CB tail characteristics energy (eV)	–	–	0.03	0.07	0.08
DOS at VB mobility edge (cm^{-3})	–	–	2×10^{21}	1×10^{22}	7×10^{21}
VB tail characteristics energy (eV)	–	–	0.045	0.08	0.09
DB concentration (cm^{-3})	–	–	5×10^{15}	8×10^{18}	2×10^{19}
DB$^{+/0}$ peak from VB (eV)	–	–	0.85	1.1	0.35
DB$^{0/-}$ peak from CB (eV)	–	–	0.7	0.5	1.2
Std. dev. of G. distribution (eV)	–	–	0.15	0.15	0.15

Note: DOS represents the density of states, CB conduction band, VB valence band, DB dangling bonds, DB$^{+/0}$ donor like dangling bond states, DB$^{0/-}$ acceptor like dangling bond states.

Please cite this article in press as: M. Mikolášek, et al., Analysis of low temperature output parameters for investigation of silicon heterojunction solar cells, Appl. Surf. Sci. (2016), http://dx.doi.org/10.1016/j.apsusc.2016.04.023

Download English Version:

https://daneshyari.com/en/article/5348110

Download Persian Version:

https://daneshyari.com/article/5348110

Daneshyari.com