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Stabilized copper plating method by programmed electroplated current: Accumulation of densely packed copper grains in the interconnect

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ABSTRACT

In this work, we programmed the plating current to stack the different size of copper (Cu) grain and analyzed the relation between the sequence of different Cu grain size and the stability of the residual stress. The residual stress was measured with varying times of annealing process in order to reach the purpose of simulating the actual Cu interconnect process. We found that varied plating strategy will make different stabilization condition of residual stress through the proof of X-ray diffraction (XRD) and optical parallel beams reflection (PBR) method. The accumulation of Cu grains, formed by Cu grain with successive variation in grain size, would enhance the packing density better than only single grain size in the finite space. The high density of the grain boundary in the electroplated Cu film will be eliminated through annealing process and it will help to suppress the void formation in further interconnect process. The electroplated Cu film with the plating current of saw tooth wave can soon reach a stable tensile stress through annealing since the Cu grains with high packing density will be quickly eliminated to approach the minimum of the strain energy which reflects to variation in the texture of Cu (2 0 0). The result of this work illustrates the importance of how to stack different size of Cu grain, for achieving a densely packed Cu film which close to the Cu bulk.

1. Introduction

While the interconnect scheme of ULSI comes down to nanoscale, the copper (Cu) grain texture study would be important to control the lowest resistance of the interconnect and the reliability performance [1]. In general, the Cu grain size and grain boundaries correspond to some physical properties, such as the residual stress [2]. Besides, the Cu grain texture would influence the stress migration (SM) [3] and electromigration (EM, reliability's key item for the interconnect quality) [4]. If the interconnect does not pass EM test, the void would be found in the interconnect [5]. The key issue to improve the reliability for nanoscale interconnect would be focused on the control of the Cu texture or grain size.

EM failure is a complex phenomenon that requires local divergence of diffusion flux [4]. While the diffusion processes along the interface, grain boundary and other paths contribute to the overall mass transport, the flux divergent sites are usually associated with localized defects. Therefore, to enhance the grain boundary density and packing density in the channel and via, and then to raise the elimination of the grain boundary only by self-annealing should be the important solution to avoid the void formation and EM failure [6].

In Cu electroplating process, the Cu grain size is strongly influenced by the plating current [7–9]. Besides, Kadota et al. reported that the dependence of grain size on the shortening of plating time was small [10]. Recent researches have shown that void defects of Cu thin films seriously degrade interconnect reliability. It is believed that good Cu film quality indeed improves void defects.

Thin film deposited on substrate is often in a state of residual stress. Stress existing in the thin film may affect a variety of the physical properties. Determination and control of the evolution of stress are important issues for thin plated Cu film. It is also a key for the yield rate in the post fabrication process of semiconductor. Thermal stability of the Cu interconnects plays a critical role in reliability performance of the ULSI semiconductor devices [11]. In fact, there are more than ten times of thermal treatment at the metallization process, and each interconnect undergoes the annealing condition of 400 °C. The stress variation of each interconnect through actual fabrication is a key solution for stability test. Large thermal stresses can be built up during the successive thermal cycling, due to the differences in the coefficient of thermal expansion for these component materials [12]. After annealing

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(or after many times of the metallization process), the residual stress leads to the stress migration and eventually causes voids in the Cu film [13]. Voids would increase the resistance and cause the product failure [14]. Therefore, how to evaluate the residual stress in the Cu interconnects is an important issue.

In our previous work, we presented an improved electroplating method to plan a simple strategy of the plating current to successfully stabilize the hysteresis stress without thermal annealing [8]. The Cu film grown by plating method is accumulated by Cu grains during the plating process. Cu grain size is strongly dependent on the amplitude of plating current. It is obvious that the residual stress is strongly influenced by stacking of Cu grain size with different grain size. This result indicated the residual stress between plated Cu film and low-k material is not constant for more thermal process, more defects and voids would be produced and the life time of the devices would be reduced.

The reduction of grain boundary energy is the main driving force for self-annealing and grain growth. When the grain size increases, the grain boundary energy decreases due to elimination of the grain boundary while the strain energy increases due to the formation of stress [15]. J. M. Paik et al. reported that the broad dihedral angle distributions meant that grain boundary energy in electroplated Cu films was anisotropic and impurities [16]. The sufficiently small grain size and strong anisotropy in the grain boundary energy of electroplated Cu films lead to abnormal grain growth observed during self-annealing [16]. The (1 1 1) texture of Cu is the closed packed plane in face-centered-cubic (fcc) structure [17]. As a result, (1 1 1) has higher electromigration resistance than other planes of the fcc structure [17]. In fcc thin films, the (1 1 1) texture is favored by the surface and interfacial energy minimization, but the (2 0 0) texture is favored by the strain energy minimization [18]. To observe the evolution of the texture of Cu(1 1 1) and Cu(2 0 0) can realize the process of the grain growth and strain development. The initial texture of the plated films is an important condition for self-annealing behavior such as reduction rate of sheet resistance and texture changes. K. Ueno et al. reported that (1 1 1) texture increases during self-annealing for the film deposited on the non-textured seed layer, but decreases on the (1 1 1) textured seed layers. This means that recrystallization behavior depends on the initial texture [19]. The initial texture is determined by the barrier layer, seed layer and the form of plating current and directly correlates to the self-annealing or sequent annealing treatment [20]. It is important for the incoming ULSI copper interconnecting technology within 10 nm [21].

In this work, we programmed the plating current to stack the different size of Cu grain and discussed the relation between the sequence of different Cu grain size and the stability of the residual stress. The residual stress of these samples was measured through times of annealing process which simulates the actual interconnect process. The accumulation of Cu grains, formed by different grain sizes successively, would enhance the interface packing density than only single grain size in the finite space. Hsiao et al. reported that the high density of nanotwins will provide high density of vacancy sinks, so no supersaturation of vacancies or nucleation of Kirkendall voids occurs [22]. The grain boundary with high density in the fresh electroplated Cu film will be easily eliminated through self-annealing process [6]. The stability of the residual stress means the Cu film is close to bulk-like and therefore the void formation is suppressed in further interconnect process. We find that varied plating strategy will make different stabilization condition of residual stress through analyses of X-ray diffraction (XRD) and optical parallel beams reflection (PBR) method. The result of this work illustrates the importance of how to stack different size of Cu grain, for achieving a densely packed Cu film which close to the Cu bulk. The accumulation of Cu grains, formed by different grain sizes successively, would enhance the interface packing density than only single grain size in the finite space.

2. Experiments

2.1. Sample preparation

Si substrates, 300-μm blanket silicon wafers, were coated with a 200-nm-thick low-k dielectric layer by plasma-enhanced chemical vapor deposition and 31.98-nm-thick TaN in sequence. The low-*k* material was black diamond. The TaN layer serves as a diffusion barrier layer and prevents copper from penetrating the low-*k* dielectric. Plasma sputtering of Cu was applied for the seed layer deposition of electro-plating.

The Cu grain size is dependent on the planting current [7]. Initially, we used the fixed plating current of 40 A to realize the variation of the residual stress under the package of the same size of Cu grain. After that, we programmed three kinds of strategical current plating, as shown in Fig. 1. The duration of each step for the strategical plating design is based on the same quantity of electrical charge. Such as the product of electric current and the duration time is constant. First type (square wave type), the strategic current is 10 A and 40 A periodically. Second type (triangle wave type), the current is set to 40 A and decreases to 10 A with the step of 10 A and then increases from 10 A to 40 A with the step of 10 A. Third type (saw tooth wave type), the current increases from 10 A to 40 A with the step of 10 A. Then, the current of 40 A rapidly drops to 10 A. The thickness of these plated Cu films is controlled around 1200 nm for comparison. Focused ion beam (FIB) cross section observation was performed. When cross-sections were prepared by FIB to observe the stack form under different programmed plating current, a protective Pt-C layer was deposited on top of the surface before milling to protect surface features [23]. Fig. 2(a), (b) and (c) shows the cross sectional FIB micrograph (Ga ion beam) for the case with programmed plating current of (a) square wave (b) triangle wave, and (c) saw tooth wave. Cross sectional FIB images of Cu plating film are hard to inspect the different size of grain distribution since Cu grains were stacked with different size by accompanying with the self-annealing effect [7].

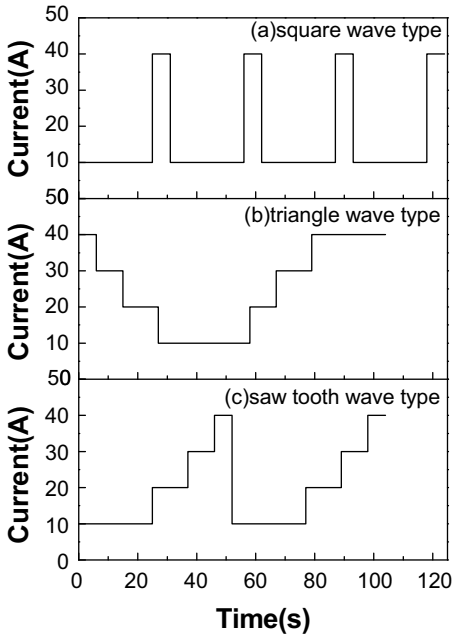

Fig. 1. Electroplated Cu film with programmed plating current of (a) square wave (b) triangle wave, and (c) saw tooth wave.

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