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Effects and mechanisms of RIE on SiC inversion layer mobility and its recovery

Gang Liu[a,*], Yi Xu[a,b], Can Xu[a,c], Alberto Basile[d], Feng Wang[e], Sarit Dhar[f], Edward Conrad[e], Patricia Mooney[d], Torgny Gustafsson[a,c], Leonard C. Feldman[a,c]

[a] Institute for Advanced Materials, Devices and Nanotechnology, Rutgers University, Piscataway, NJ 08854, USA
[b] Dep't. of Chemistry and Chemical Biology, Rutgers University, Piscataway, NJ 08854, USA
[c] Dep't. of Physics & Astronomy, Rutgers University, Piscataway, NJ 08854, USA
[d] Dep't. of Physics, Simon Fraser University, Burnaby, BC V5A 1S6, Canada
[e] School of Physics, The Georgia Institute of Technology, Atlanta, GA 30332, USA
[f] Physics Dep't, Auburn University, Auburn, AL 36849, USA

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ABSTRACT

We report the use of hydrogen annealing to implement the substantial recovery of the a-face $(1\,1\,\bar{2}\,0)$ crystal structure and the 4H SiC MOSFET inversion layer mobility following material degradation by reactive ion etching (RIE). The results impact the processing of SiC trench MOSFETs where the a-face sidewall forms a significant portion of the conducting semiconductor channel.

1. Introduction

The need for high power, high temperature, and energy saving electronics has led to increased interest in wide band gap MOSFET type devices. Enhancement in the crystal quality of 4H-SiC and significant advances in processing technology suggest that such a MOS based technology can be realized using this semiconductor material. The trench MOSFET (or U MOSFET) is a desirable device design for next-generation SiC power MOSFET due its higher current density than the conventional double-implanted or D-MOSFET structure [1]. Trench devices usually employ the Si-face or C-face of a SiC wafer, with trench side walls, typically formed by Reactive Ion Etching (RIE). The side walls may correspond to crystalline a-faces, including the $(1\,1\,\bar{2}\,0)$ face. This particular crystal face yields higher mobility than the Si-face, given the same post oxidation anneal [2–6]. UMOSFETs formed by RIE with high mobilities have been reported [7] [8] [9]. However, RIE enhances surface roughness and creates defects in the epi layer that tend to degrade the device. An early report of a high voltage UMOSFET formed with an RIE trench found severe roughness on the sidewall after RIE as measured by AFM. The roughness was not substantially reduced after sacrificial oxidation [10]. One solution to the roughness issue is etching in an H_2 environment at elevated temperatures. This process has been shown to be effective in improving surface morphology after RIE and has been used to create flat surfaces, on Si-face, C-face and other faces [11–13].

In addition to morphology degradation Kawahara et al. [14] has shown that on the Si-face, RIE induced defects exist in the SiC epi through many microns in depth, detected by Deep Level Transient Spectroscopy (DLTS). As well, dopant deactivation accompanied the RIE process. It was reported that doping deactivation and defect density can be reduced by thermal oxidation, and some of the remaining defects could be further reduced by subsequent 1400 °C anneal in Ar, although all of the detectable defects could not be completely removed by these processes.

In this work we build on these early results and explore these RIE-induced detrimental effects on SiC a-face MOSFETs. We address the following specific questions: (i) What is the RIE impact on the a-face in terms of surface roughness and defects in the epi layer? (ii) How does the RIE induced roughness and accompanying defects affect the MOS structure, including breakdown and inversion carrier mobility? (iii) What is the effect of post RIE H_2 etching on defect reduction? (iv) Can an H_2 etch recover a high performance a-face MOSFET?

* Corresponding author.
E-mail address: gliu82@yahoo.com (G. Liu).

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The main result of this work shows that an H_2 etch substantially recovers the performance of post-RIE a-face MOSFET. The inversion layer mobility is not fully recoverable, possibly due to relatively higher interface defect density and residual RIE induced defects in the near interface epi layer. Electrical probes and materials analysis studies indicate the underlying mechanisms that accompany the damaging process and the subsequent recovery.

2. Experiment

Using a well-cut, a-face, 4H SiC wafer with a p-type epitaxial layer (Al doping $\sim 1 \times 10^{16}\,cm^{-3}$), n+ source and drain areas were formed by nitrogen implantation at 700 °C with different energies and doses, to form a box profile into SiC with n-type doping of $6 \times 10^{19}\,cm^{-3}$. The implanted nitrogen is then activated and the implantation damage annealed thermally at 1550 °C for 30 min in an Ar ambient, with the surface protected by a graphite cap. After annealing, the cap is removed by an O_2 plasma etch. A thick sacrificial oxide is then grown to recover the surface from any negative effects caused by the previous processes.

Device fabrication for channel mobility evaluation included the following steps: (i) RCA cleaning, (ii) thermal oxidation in pure O_2 at 1150 °C for 1 h to a thickness of ~50 nm, (iii) a 2 h NO anneal at 1175 °C, resulting in a total gate oxide thicknesses of ~55 nm. (Note, in most cases in this paper, the well-established post-oxidation NO process for high mobility is employed to passivate the oxide/semiconductor interface defects that exist regardless of RIE. This both provides greater sensitivity to any residual defects and fits the conventional practice.) The source and drain areas were then exposed by HF etching of the sacrificial oxide and Al was deposited and patterned to form ohmic contacts. Finally the gate contact was formed by patterned Al deposition.

MOS capacitors (MOSCAP) are formed on an n-type companion sample fabricated at the same time with the identical oxidation and NO anneal steps for interface state density (D_{it}) evaluation,. The MOSCAP's were formed by Al deposition and patterning on the gate oxide. Deposited Al was used as an ohmic contact on the back of the sample after oxide removal by HF. Electrical measurements were carried out to extract field effect mobility on MOSFETs and D_{it} from MOSCAPs.

After initial electrical testing, all electrode metals were removed by wet etching, and the gate oxide was removed by HF, exposing the interface surface. Atomic Force Microscopy (AFM) measurements were carried out in the channel regions and on companion samples.

The same samples were then exposed to an RIE process, with SF_6 10 sccm, Ar 40 sccm, RF150 W, DC self-bias 250 V, pressure 60 mTorr, at room temperature and a plasma time of 1 min. Approximately 70 nm of SiC is removed by this process. After RIE, the oxidation/NO fab process was repeated on the "as-etched" surface to produce MOSFETs and MOSCAPs for mobility and interface state density measurement. Following this second round of electrical testing, the oxide was completely etched for another AFM scan.

The RIE roughened surfaces were then subjected to a 1400 °C H_2 (2.9% hydrogen in argon, 1 slm) etch process, for 5 min at peak temperature. FTIR shows this removes approx. 100 nm of SiC. After AFM evaluation, we repeated the device fabrication and electrical testing procedure described above.

Physical characterization of large area companion samples processed under the same conditions was determined using X-ray photoelectron spectroscopy (XPS), medium energy ion scattering (MEIS) and atomic force microscopy (AFM). The complete processing and characterization flow is summarized in Diagram 1.

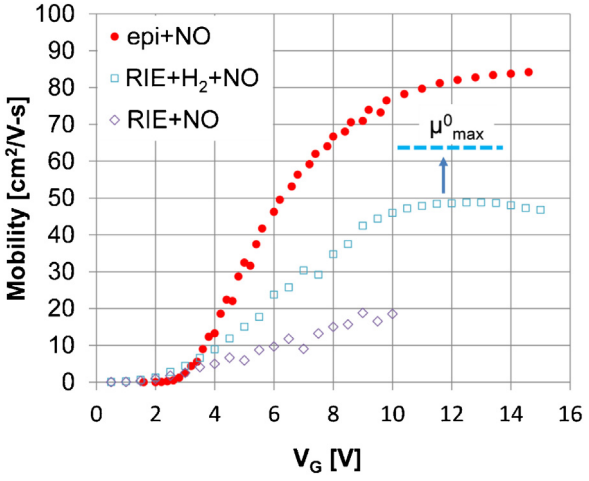

Fig. 1. Field effect mobilities for 4H-SiC MOSFETs with 2 h standard NO anneal, beginning with: peak $\mu_{FE} = 85\,cm^2/V\,s$ on epitaxial surface, then reduced to $\mu_{FE} = 20\,cm^2/V\,s$ after RIE process and recovered to $\mu_{FE} = 64\,cm^2/V\,s$ after an H_2 etch. μ^0_{max} is the contact resistance corrected peak mobility for RIE + H_2 + NO sample.

3. Results

Fig. 1 shows field effect mobilities comparing the epitaxially grown surface with surfaces that have undergone RIE and H_2 processing. Clearly the RIE process reduces the mobility extensively and the H_2 etch significantly recovers mobility, although not completely. In addition to lower mobility, the RIE devices show lower yield and early gate oxide breakdown.

After an H_2 etch, although the source and drain contacts are still ohmic, the resistance increased by 3 orders of magnitude, to as high as $1\,\Omega\,cm^2$, according to Transmission Line Model (TLM) measurements. This can be due to the multiple oxidations, RIE and H_2 etch processes on the same SiC consuming significant portions of the implanted n+ SiC regions that are essential for ohmic contact. As a result, the evaluated field-effect mobility is substantially underestimated using this formula, $\mu_{FE} = (L/WC_O V_{DS})(dt_D/dV_G)\big|_{V_{DS}\to 0}$, since the real channel voltage is considerably smaller than V_{DS}. However given the total effective conductance of the device and source-drain series resistance, the intrinsic maximum field effect mobility μ^0_{max} for RIE + H_2 + NO sample can be conveniently corrected [15], as marked in Fig. 1.

To understand the origin of these differences, physical and electrical analysis methods were combined to study to these structures.

Atomic force microscopy (AFM) was used to examine roughness and correlate with the measured mobility. Fig. 2 shows that the initial atomically flat surface is significantly roughened by RIE, and thermal oxidation that grows 55 nm oxide cannot recover the surface. An H_2 etch is confirmed to be very effective in recovering the RIE roughened surface to the epi-like condition, consistent with earlier reports [13]. The corresponding RMS values are 0.25 nm, 4.57 nm and 0.28 nm for epi, RIE and RIE + H_2 etched samples respectively. The different resulting surface roughness between oxidation and H_2 etch may be due to their distinct etching mechanisms. The H_2 etch process removes Si and C through Si sublimation at high temperature, and CH_x gas phase products. The rough features have more dangling bonds, with higher reaction probability thus faster etching rate [16]. Such selective etching results in a flat surface. Oxidation also consumes SiC, but it forms a SiO_2 layer, resulting in interface that is mostly conformal to the initial morphology.

Medium energy ion scattering (MEIS) combined with channeling is a materials characterization technique that is sensitive to structural imperfections of a surface, particularly near-surface