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Effective surface passivation of p-type crystalline silicon with silicon oxides formed by light-induced anodisation

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ABSTRACT

Electronic surface passivation of p-type crystalline silicon by anodic silicon dioxide (SiO_2) was investigated. The anodic SiO_2 was grown by light-induced anodisation (LIA) in diluted sulphuric acid at room temperature, a process that is significantly less-expensive than thermal oxidation which is widely-used in silicon solar cell fabrication. After annealing in oxygen and then forming gas at 400 °C for 30 min, the effective minority carrier lifetime of 3–5 Ω cm, boron-doped Czochralski silicon wafers with a phosphorus-doped 80 Ω/□ emitter and a LIA anodic SiO_2 formed on the p-type surface was increased by two orders of magnitude to 150 μs. Capacitance–voltage measurements demonstrated a very low positive charge density of 3.4×10^{11} cm^{-2} and a moderate density of interface states of 6×10^{11} eV^{-1} cm^{-2}. This corresponded to a silicon surface recombination velocity of 62 cm s^{-1}, which is comparable with values reported for other anodic SiO_2 films, which required higher temperatures and longer growth times, and significantly lower than oxides grown by chemical vapour deposition techniques. Additionally, a very low leakage current density of 3.5×10^{-10} and 1.6×10^{-9} A cm^{-2} at 1 and −1 V, respectively, was measured for LIA SiO_2 suggesting its potential application as insulation layer in IBC solar cells and a barrier for potential induced degradation.

1. Introduction

Thermally grown silicon dioxide (SiO_2) has been widely used to electronically passivate surfaces of silicon solar cells over the past few decades. The resulting high quality silicon–SiO_2 interface enables surface recombination velocity's (SRV) less than 30 cm s^{-1} [1] to be achieved. This has resulted in these films being used extensively in high efficiency silicon solar cell fabrication [2–4]. Thermal SiO_2 has also found application as a barrier layer under silicon nitride (SiN_x) antireflection coatings of silicon solar cells, which effectively avoids over-plating of metal through pinholes in the SiN_x [5]; a contact passivation layer [6–9] and can mitigate potential induced degradation (PID), where minimising leakage current through the antireflection coating is paramount [10]. However, the growth of thermal oxides requires long oxidation times and high temperatures, which can reduce minority carrier lifetimes in silicon wafers through thermal stress, oxygen precipitation or contamination during the high temperature process. The significant thermal budget incurred in forming thermal oxides is not compatible with the trend of reducing manufacturing cost in the photovoltaic industry. Therefore the development of alternative techniques of oxidation at low temperatures is of great significance.

Several low-temperature oxidation processes have been developed, which have resulted in good surface passivation (see Table 1). These include chemical vapour deposition (CVD) processes, such as plasma enhanced CVD (PECVD) [11–13], atmospheric pressure CVD (APCVD) [14,15] and expanding thermal plasma (ETP) technique [16]. While CVD techniques have demonstrated SRVs less than 100 cm s^{-1}, the reactors used in these deposition systems require a large amount of maintenance and the precursors used to form SiO_2 are both dangerous and expensive.

Alternatively, SiO_2 can be grown by immersing silicon wafers in an oxidising solution (e.g., nitric acid (HNO_3) [10–12]). Grant et al. reported a SRV of 42 cm s^{-1} by growing SiO_2 in 70% (w/w) HNO_3 followed by a 1000 °C anneal in nitrogen and a subsequent forming gas anneal at 400 °C [17]. Although the SRV was low, the advantage

Abbreviations: CV, capacitance–voltage; CVD, chemical vapour deposition; Cz, Czochralski; ETP, expanding thermal plasma; LIA, light-induced anodisation; MOS, metal-oxide-semiconductor; PID, potential induced degradation; QSS-PL, quasi steady state photoluminescence; SRV, surface recombination velocity.

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Table 1
A summary of the SRV of SiO_2 formed by different techniques.

Ref.	Oxidation technique	Deposition temp, (anneal temp), ambient	SRV ($cm\,s^{-1}$)
[1]	Thermally-grown	1050 °C, (450 °C), forming gas	30
[12]	PECVD	350 °C, (400 °C), forming gas	500–1300
[15]	APCVD	400 °C, (400 °C), forming gas	1.2×10^5
[16]	Expanding thermal plasma (ETP)	400 °C, (600 °C), forming gas	54
[17]	Chemical oxidation in nitric acid	108 °C, (1100 °C), nitrogen	107
[17]	Chemical oxidation in nitric acid	108 °C, (1100 °C), nitrogen and (400 °C), forming gas	42
[20]	Immersed anodisation (DC bias)	25 °C, (400 °C), O_2 and forming gas	35
[18]	Immersed anodisation (AC bias)	25 °C, (400 °C), O_2 and forming gas	15

of a low temperature wet chemical oxidation was mitigated by a slow oxidation rate and the requirement for a high temperature anneal.

Recent developments in the formation of SiO_2 by anodisation have enabled relatively fast oxide growth rates at room temperature. It has been demonstrated after annealing in oxygen and forming gas at 400 °C, the anodic SiO_2 formed with DC and AC bias attained a very low SRV of 35 and 15 $cm\,s^{-1}$ [18], respectively. The light-induced anodisation (LIA), first reported by Cui et al. [19], can result in faster oxide growth and increased uniformity. Similarly to [18], once annealed in oxygen and forming gas at 400 °C, the LIA SiO_2 passivated wafers achieved comparable effective minority carrier lifetimes (hereafter effective lifetime) to the as grown thermal SiO_2. In this paper, we investigate the passivation of p-type silicon surfaces by anodic SiO_2 formed by LIA after annealing in oxygen and forming gas at 400 °C for 30 min. Photocouductance and quasi steady state photoluminance (QSS-PL) measurements were conducted to determine the effective lifetime and an upper limit to the SRV. Capacitance–voltage (CV) measurements are performed to assess the charge density (Q_{eff}) associated with the anodic oxide and the density of interface states (D_{it}) at the silicon–SiO_2 interface.

2. Experimental

2.1. Sample preparation

Anodic SiO_2 films were prepared on alkaline-textured 3–5 Ω cm p-type Czochralski (Cz) silicon ~16 cm^2 wafers of a thickness of 180 μm and with a $POCl_3$-diffused emitter sheet resistance of 80 Ω/□. The p-type surfaces of the wafers were planarised by etching in 25% (w/v) sodium hydroxide (NaOH (J.T. Baker)) at 80 °C for 7 min. A layer of thermal SiO_2 of 18 nm thickness on both surfaces was grown by dry oxidation at 950 °C for 18 min in a quartz tube furnace. After oxidation, the p-type surface of the wafers were single-side etched in 1% (w/v) HF for 2 min to remove any native oxide on the surface before LIA SiO_2 formation and annealing.

The LIA SiO_2 growth was performed in 0.5 M H_2SO_4 (BASF VLSI, where trace metal levels are typically less than 100 ppb) for 15 min as described in [19], which resulted in an anodic SiO_2 layer of 23 nm thick. A constant illumination of 180 W m^{-2} was provided by an array of 23 W compact fluorescent light bulbs at a distance of 5 cm from the n-type surface of the wafer. The wafers were anodised under constant positive bias of 15 V, which offset the series resistance in the electrochemical circuit and controlled the operating point of the solar cell close to short circuit. After anodisation, the wafers were annealed in a quartz tube furnace at 400 °C. In order to identify the most effective annealing condition to achieve the best surface passivation, the samples were annealed in either oxygen, forming gas or both. Wafers processed in the above mentioned manner were characterised by X-ray photoelectron spectroscopy (XPS) and transmission electron microscopy (TEM) and published in [19].

To perform CV measurements, the thermal SiO_2 was removed from the n-type surface via HF fuming, and 150 nm of aluminium was thermally evaporated onto the rear surface to enable electrical contact to the silicon wafer. Finally, circular Al contacts with a diameter of 0.70 mm were evaporated on the front surface to complete the metal-oxide-semiconductor (MOS) structures.

2.2. Characterisation

The effective minority carrier lifetime, τ_{eff}, of the wafers were measured after thermal oxidation and after the post anodisation anneal to enable a direct comparison of surface passivation between the thermal SiO_2 and the anodic SiO_2. Photoconductance measurements were performed using a lifetime tester (WCT-120 from Sinton Instruments) under quasi-steady-state illumination and the generalised analysis [21]. Since QSS-PL measurements are not affected by depletion-region modulation [22,23], accurate τ_{eff} data at low injection levels was acquired. QSS-PL was conducted on a modified Sinton Instruments WCT-120, which enabled simultaneous measurements of the excess conductance, the photoluminescence intensity, and the generation rate [24].

The wafers used for lifetime measurements contained a phosphorus-diffused emitter on one surface, so the measured τ_{eff} contains contributions from bulk recombination, surface recombination and emitter recombination, and can be represented by:

$$\frac{1}{\tau_{eff}} = \frac{1}{\tau_{bulk}} + \frac{1}{\tau_{surface}} + \frac{1}{\tau_{emitter}} \quad (1)$$

where the bulk recombination lifetime τ_{bulk} was measured by a HF passivation method [25], and the emitter recombination lifetime $\tau_{emitter}$ at high injection levels was described by Eq. (2) [26]:

$$\frac{1}{\tau_{emitter}} = J_{0e}\frac{\Delta n}{qWn_i^2} \quad (2)$$

where J_{0e} was the emitter dark saturation current, W was the thickness of the wafer, n_i was intrinsic carrier concentration, and Δn was the minority carrier concentration. The surface recombination lifetime was then determined by solving $\tau_{surface}$ in Eq. (1) and the upper limit of the SRV on the p-type surface can then be calculated by Eq. (3) with a high level of accuracy [27]. The τ_{eff} and SRV values for LIA anodic SiO_2 reported in this paper are measured/calculated at an injection density of $\Delta n = 10^{15}$ cm^{-3}.

$$\mathrm{SRV} \leq \frac{W}{\tau_{surface}} \quad (3)$$

Capacitance–voltage measurements were performed at high frequency (1 MHz) using a 4284A Precision LCR meter and at low frequency using a 4014B pA meter. From these measurements, Q_{eff} was determined from the flat band voltage of the high frequency curves, while the D_{it} was calculated using the Terman [28] and Castagne [29] methods, with the latter technique being the more accurate.