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## Applied Surface Science

journal homepage: [www.elsevier.com/locate/apsusc](http://www.elsevier.com/locate/apsusc)



## A feasibility study for controlling self-organized production of plasmonic enhancement interfaces for solar cells

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### ARTICLE INFO

#### Article history:

Received 31 October 2013

Received in revised form

14 December 2013

Accepted 15 December 2013

Available online xxx

#### Keywords:

Plasmonics

Solar cells

Dewetting

Silver nanoparticles

### ABSTRACT

The decoration of metal nanoparticles (MNPs) by the self-organized mechanism of dewetting is utilized as a suitable method for plasmonic interface integration to large area full-scale solar cell (SC) devices. Reflection measurements are performed on both flat and textured silicon (Si) SCs in order to investigate the local plasmonic resonances of the MNPs. The effects of particle size and thickness of silicon nitride (Si<sub>3</sub>N<sub>4</sub>) anti-reflection coating layer are investigated by reflection measurements and the shift of plasmon resonance peak position. It is found that surface roughness, annealing time, annealing temperature, and varying Si<sub>3</sub>N<sub>4</sub> thickness can be used as mechanisms to control the size distribution, shape of the resultant nano-islands, and SC efficiency. The findings on the most suitable nanoparticle system production parameters by this method, depends on the applied substrate properties which are expected to guide further applications of plasmonic interfaces and also to the other kinds of device structures in the ultimate quest for attaining affordable high efficiency SCs.

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### 1. Introduction

Plasmonic enhancement interfaces for SCs are layers made of nanometer scale continuous or dispersed conductive materials bearing high concentration of free charge carriers incorporated into the structure of a conventional bulk or thin film SCs which are used for facilitating enhanced light absorption into the active region of a SC. The mechanism of enhancement primarily relies on increased optical path length of incident photons in the active region due to strong scattering of light from the free charges, typically electrons, to the highly conductive-typically noble metal-material. These plasmonic enhancement interfaces can be regarded as light trapping layers giving rise to better photon management in an analogy to photonic structures but with a major difference in the scale of layer dimension. The difference of the size is due to the fact that photons incident on metal structures can couple strongly to collective charge oscillations, the plasmons, and become plasmon polaritons. Trapping of light (helping light to stay longer in the active region of SC) can lead to affordable SCs with high

efficiency by increasing the absorption and generating more photocurrent. The two main ingredients of nano-photonic light trapping for SCs are plasmon polaritons which are coupled photons with collective oscillations of free electrons in noble metals, and high-refractive-index dielectrics which introduce resonance phenomena at particular frequency that gives rise to pronounced scattering and impedance matching capabilities. Plasmonic SC is one of the emerging SC technologies to enhance the optical absorption. Light trapping is important factor for achieving higher energy conversion efficiency as the light travels longer distance within the active layer. However, without plasmonic nanoparticles (NPs), incident light will be partially reflected back and path length will be the thickness of the substrate. The scattering efficiency of NPs depends on the particle size, refractive index of underlying, and surrounding environment. There are different MNPs with various scattering efficiency. In this study, silver (Ag) is used as MNPs because of the low absorption coefficient and the superior optical extinction properties than the other metals in the visible spectrum of light [1–4]. Silver NPs (AgNPs) lead to increase the light scattering into the substrate.

MNPs can be used in two basic mechanisms in photovoltaic (PV) applications which affect the far and near fields. Far-field effect consists of light scattering from the metal particles into the active layer of SC which behave as dipole, whereas near-field effect is the field enhancement in the vicinal surrounding of MNPs.

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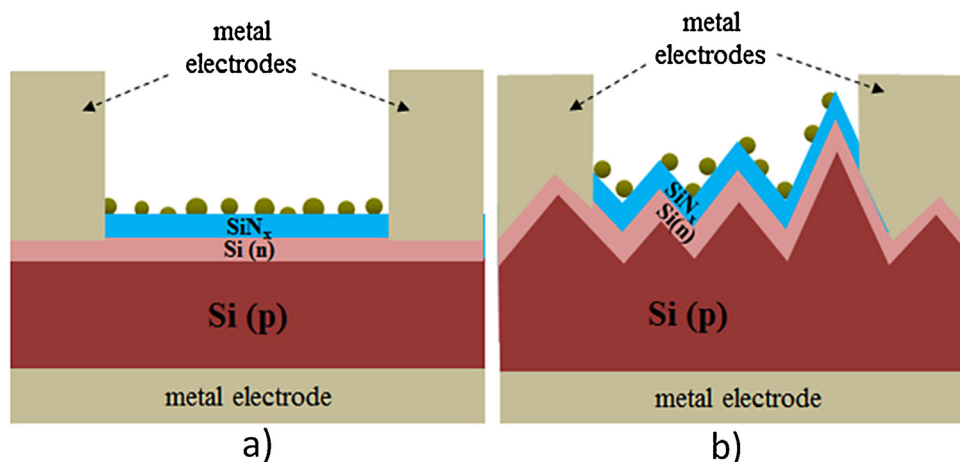


Fig. 1. Sketch of the devices: (a) flat, (b) textured.

Both flat and textured bulk Si SCs are investigated in the full scale. Both kinds of cells are fabricated in multiplicity with varying dielectric anti-reflection coating (ARC) thickness. The studied plasmonic interfaces are fabricated by using the self-organized process of surface dewetting due to the ease of application, ease of integration to the state-of-the-art bulk SC production facility, and most importantly for its low-cost. In this technique, initially a several nanometer thick continuous Ag film is deposited on a desired surface of choice and the SC is thermally treated at elevated temperatures such that the atoms comprising the continuous Ag film starts to diffuse and form holes, and dewet the surface. These holes in the Ag layer eventually merge giving rise to formation of liquid droplet shaped metal islands of a few to several tens of nanometer large sizes. As the process continues, small islands tend to disappear and the larger ones tend to grow in size by acquiring the atoms of the smaller ones depicting a morphological coarsening process similar to Ostwald ripening [5].

Texturing Si SC, the high surface roughness of substrates increases the multiple reflections. Light trapping is a factor for improving the current density and cell efficiency. However, the addition of plasmonic NPs on textured Si SC can be parasitic and result in large optical loss during multiple reflections. The presence of the AgNPs cause both scattering and absorption of incoming light. However, the effect of absorption cannot be denied as compared to the scattering. This absorption blocks the second order reflections from the surface of textured Si SC. Therefore, this situation causes the decrease in the efficiency of SC, while in flat Si SC with low roughness and smooth substrate; plasmonic NPs themselves can introduce excellent light trapping that leads to the improvement of the current density and increases the cell efficiency with respect to the devices without NPs [6–12]. Fig. 1 shows a sketch of flat and textured crystalline Si (c-Si) SCs, in panel 1a and 1b, respectively.

## 2. Experimental details

Step-by-step description of SC device fabrication is summarized by the texturing,  $\text{Si}_3\text{N}_4$  deposition, metallization, edge isolation, and the self-organized fabrication method called surface dewetting as shown in Fig. 2.

### 2.1. Fabrication of monocrystalline silicon solar cell

Saw damage etching is the first step which is performed before production of the mono c-Si SC. The c-Si is grown as ingots are commonly produced by Czochralski technique after they are cut into thin wafers. During the cutting process, the surface of the Si

ingot is damaged from the sawing of wafers. A concentration of 20% KOH at 80 °C is used to remove shallow cracks and surface defects on the surface of the thin Si wafers.

Surface texturing is the next step which is used to reduce the reflection of light away from the substrate and to improve the light absorption which leads to enhance the amount of light converted into photocurrent in Si SCs. p-type Si surfaces are textured by wet anisotropic KOH chemical etching technique. The pyramid structures created on the surface of the SCs lead to multi reflection of incident light from the surface.

For construction of solar cell, the p–n junction is formed inside the semiconductor materials. p–n junction was created by diffusion of phosphorus into the p-type Si wafer which is doped with Boron. The process is performed by thermal physical vapor deposition (PVD) system at 850 °C for 200 sccm  $\text{POCl}_3$  flow. During the doping process, the deposited n-layer covers all of the substrate which includes both the edges and back side of the wafer. The front and back contacts that are connected by deposition of n-layer around the edge lead to create shunt current and recombination of separated electron-hole which reduced SC operation [13]. Therefore, to remove shunt current, the edges of the wafer are isolated by laser scribing. The cell performance of a SC decreases by reflection of incident light from the Si surface. In this work,  $\text{Si}_3\text{N}_4$  as an ARC layer at different thicknesses is deposited by plasma enhanced chemical vapor deposition (PECVD) system. In metallization process, the metal contacts are created in front and back side of the solar cell to transport the charge carrier's separation to an external load. In this study, Ag paste is used for front grid metallization contact and aluminum paste is coated fully for the back metallization contact. The pastes are deposited by screen-printing on the device. After deposition of Ag/Al pastes as metal contacts, all devices are exposed to firing step under high temperatures due to induce the metal

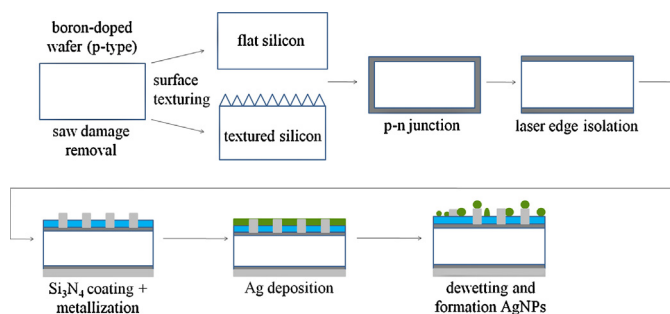


Fig. 2. The production steps of mono c-Si SC and fabrication of MNPs.

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