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Effect of reactive magnetron sputtering parameters on structural and electrical properties of hafnium oxide thin films

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Abstract:

The purpose of this work was to compare the structural and electrical properties of magnetron sputtered hafnium oxide (HfO_x) and hafnium oxynitride (HfO_xN_y) thin films. A careful analysis of the influence of deposition process parameters, among them: pressure in the reactor chamber, Ar and O_2 flow rate, power applied to the reactor chamber and deposition time, on electro-physical properties of HfO_x and HfO_xN_y layers has been performed. In the course of this work we performed number of experiments by means of Taguchi's orthogonal arrays approach. Such a method allowed for the determination of dielectric layers properties depending on process parameters with relatively low amount of experiments. Moreover, there has been also reported effects of post-deposition annealing on electrical characteristics of metal–insulator–semiconductor (MIS) structures with HfO_x or HfO_xN_y gate dielectric and its structural properties. Investigated hafnia thin films were characterized by means of spectroscopic ellipsometry (SE), electrical characteristics measurements, Atomic Force Microscopy (AFM), X-ray Diffraction Spectroscopy (XRD) and Rutherford Backscattering Spectrometry (RBS).

Highlights

- Structural and electrical characterization of HfO_x and HfO_xN_y thin films.
- Analysis of the influence of deposition process parameters on properties of dielectric films.
- Investigation of the post-deposition annealing on HfO_x and HfO_xN_y properties.
- Experiment has been designed with the use of Taguchi's orthogonal arrays.
- The most favorable annealing temperature of HfO_x and HfO_xN_y is 300°C.

Keywords: Hafnium oxide, Magnetron sputtering, Structural properties, Electrical characterization

1. Introduction

Ongoing development of the microelectronics, starting from the early 60s` of the 20th century, involves an increase in the integration degree of emerging semiconductor devices, as well as the increase of speed and functionality of integrated circuits (ICs). The scaling of complementary metal-oxide-semiconductor (CMOS) feature size has also caused a decrease