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Properties of HfO_2/ultrathin SiO_2/Si structures and their comparison with Si MOS structures passivated in KCN solution☆

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ABSTRACT

Electrical, optical and partly structural properties are investigated on very thin ALD HfO_2/ultrathin NAOS SiO_2/n-type Si structures. An ALD layer was deposited at 250 °C and it contains amorphous and crystalline–probably monoclinic HfO_2 phases. HfO_2 films with both types of structural phases were not stable if thermal treatment above 200 °C was applied. On as- prepared samples, deep interface traps with activation energy of $\Delta W = 0.23$ eV have been determined. After annealing of the structure at 200 °C, the traps were partly transformed and a mid-gap level $\Delta W = 0.49$ eV was detected. FTIR and AFM measurements confirmed presence of HfO_2 monoclinic phase in the HfO_2 films. On the other side, the density of interface defect states of the structure decreased from approx. 10^{12} eV^{-1} cm^{-2} to 10^{11} eV^{-1} cm^{-2} after low temperature annealing of the reference structure. The results are compared with very similar (almost identical) development of interface defect states on the very thin thermal SiO_2/Si structure before and after passivation in a 0.1 M KCN methanol solution.PACS: 78.55.Qr; 78.66.Jg; 81.16.Pr; 85.40Ls

1. Introduction

Many contributions have been devoted to investigation of HfO_2/SiO_2/Si structures because high-k materials offer unique possibilities in the field of Si-based device miniaturization. Barret et al. [1] analyzed thermal stability of such structures. Tan et al. [2] published comparative study of interfacial characteristics of sputter-deposited hafnium dioxide (HfO_2) on native SiO_2/Si. The same author, Tan et al., published a paper [3] about preparation of high-quality ultrathin HfO_2 films and about comparison of HfO_2/SiO_2/Si structures. We are using term "ultrathin layer" for film of thickness less than 2.5 nm. Term "very thin" is used for thickness of films between 2.5 and 10 nm. Term "thin" layer is used for thickness above 10 nm.

Taube analyzed fabrication and characterization HfO_2 films [4]. More authors devote their attention to structures HfO_2/SiO_2/SiC, e.g., in [5–9]. Alles et al. [10] published formation of monoclinic HfO_2 films by two step process where the initial growth of about 1 nm at 170 °C was continued up to 10–30 nm at 300 °C. This process formed uniform, monoclinic HfO_2 films with RMS roughness of 1.7 nm for 10–12 nm thick films. An 11 nm thick HfO_2 film deposited onto bilayer substrate (graphene) reduced the electron mobility by less than 10% at the Dirac point and by 30–40% far away from it. Monoclinic HfO_2 films were investigated by Raman spectroscopy in more laboratories. Alles et al. [10], Lixin Liu et al. [11] presented one of dominant peak in Raman spectra related to monoclinic HfO_2 at 496 cm^{-1}. This peak is assigned to the A_g strongest vibration mode of monoclinic HfO_2 [12]. Formation of a SiO_2 interlayer and its properties have important role in successful formation of HfO_2/SiO_2/Si structures suitable for device fabrication. Japanese scientists–ISIR of Osaka University–developed during years 1998–2013 technology of formation of high-density ultrathin SiO_2 layers by wet chemical oxidation in an HNO_3 solution of high concentrations, see e.g., [13–20]. The used abbreviation of this process is NAOS–nitric acid oxidation of semiconductors. Kim et al. [21] published formation of ultrathin SiO_2 layer with low leakage current density with ~100% nitric acid vapor. The vapor generated by boiling of HNO_3 solution was introduced into quartz glass tube and oxidation was performed at 100–200 °C. In the paper is presented also corresponding phase diagram of the nitric acid and water system for concentration of HNO_3 from 0 to 100%. Si oxidation in HNO_3 vapor proceeds by following reactions:

$$2HNO_3 \rightarrow NO_2 + NO + H_2O + 2O$$

$$Si + 2O \rightarrow SiO_2$$

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Table 1
List of prepared samples.

Name	Mode of NAOS	Temperature of Si sample at ALD	Thermal annealing
Sample No. 1	100% HNO_3 vapor	250 °C	As prepared
Sample No. 2	100% HNO_3 vapor	250 °C	200 °C 10 min
Sample No. 3	100% HNO_3 vapor	250 °C	300 °C 10 min
Sample No. 4	100% HNO_3 vapor	250 °C	400 °C 10 min

Sample No. 1: as prepared $HfO_2/SiO_2/Si$; Sample No. 2: $HfO_2/SiO_2/Si$ annealed in N_2 at 200 °C, 10 min.
Also samples annealed at 300 °C (Sample No. 3) and 400 °C (Sample No. 4) in N_2 for 10 min were prepared and results will be partly presented and discussed in the paper.

Diffusion of oxidizing species–mainly oxygen atoms–is the rate-determining step. When the SiO_2 layer is formed with high concentration HNO_3, its atomic density is higher than that formed with less concentrated HNO_3. Authors are stating that ultrathin SiO_2/Si structures have low interface state density, especially after the post-metalization annealing at 250 °C in inert atmosphere with 5 vol% of hydrogen and also the low concentration of suboxide species.

The research works of Slovakian laboratories from above mentioned field of NAOS samples have been published in e.g., [23–25]. Bury et al. [26] published results obtained on $HfO_2/SiO_2/Si$ structures with similar composition and technology as it is presented in this work. The present authors used acoustic version of DLTS for measurements and determination of corresponding electrical parameters.

The dominant aim of this work is to present application of high-density ultrathin NAOS SiO_2 prepared in 100% HNO_3 vapor as an interlayer between the Si substrate and the high-k HfO_2 overlayer deposited by the ALD and to discuss advantages and/or disadvantages of such structure.

2. Experiment–preparation of samples

2.1. Preparation of $HfO_2/SiO_2/Si$ structures

A very thin HfO_2 layer of 5 nm thickness was prepared by atomic layer deposition (ALD) from TDMAH: tetrakis(dimethylamino) hafnium - $Hf[N(CH_3)_2]_4$ in oxidant water steam at 250 °C. The ALD HfO_2 layer used in presented experiments contains amorphous and crystalline–probably monoclinic phases. This fact will be confirmed in the next parts.

A SiO_2 interlayer of thickness approx. 0.6 nm between HfO_2 and c-Si was formed in 100% HNO_3 vapor by technology described in Kim et al. [21]. The metal-oxide-semiconductor (MOS) structure was fabricated from P-doped n-type Si(1 0 0) wafers. The Si wafers were cleaned using Radio Corporation of America (RCA) method followed by etching with dilute hydrofluoric acid. List of prepared samples is presented in Table 1.

2.2. Preparation and KCN passivation of thermal very thin SiO_2/Si structures

Results obtained on the set of samples described in the Table will be compared with corresponding results presented in Pincik et al. [25]. Structure of samples is very thin thermal SiO_2/n-Si(100). We will compare results with as prepared samples (at 800 °C) and with passivated in boiling 0.1 M solution of potassium cyanide (KCN) in methanol for 2 min. SiO_2 thickness is ~7.4 nm.

3. Experimental methods

For investigation of electrical properties of prepared structures in the form of metal-oxide-semiconductor (MOS), the following methods were used: charge version of deep level transient spectroscopy (Q-DLTS), measurements of capacitance vs. voltage in time domain (C–V), Fourier transform infrared spectroscopy (FTIR), IR reflectance, and atomic force microscopy (AFM).

3.1. Charge version of deep level transient spectroscopy (Q-DLTS)

The modified charge-based correlation DLTS method was used to study prepared MOS structures. The equipment with corresponding software has been developed in Institute of Physics SAS, Bratislava, Slovakia [22] and commercial type does not exist. Therefore, it is needed briefly to describe it. This method is based on the correlation approach, i.e., the transient response of the MOS structure under periodically applied voltage steps to the gate electrode is measured, and subsequently a weighted combination of the charge signals obtained at various sampling events is achieved. The sampling events, as well as the weighting coefficients used in our work, are chosen with the aim to improve the selectivity in the measured spectra. The resulting correlated charge DLTS signal is described by a weighted summation of the contributions from three channels. The parasitic output charge due to the presence of a leakage current is eliminated by the used filtering scheme.

The following formula is valid for the measured Q-DLTS signal coming from a deep trap:

$$\Delta Q \approx \left[\frac{C_{ox}}{C_{ox}+C_s}\right] q \times w \times N_T \times \exp(-e_n t), \tag{1}$$

where w stands for the excited part of the depletion region, e_n is the emission rate of the traps, N_T for the trap density, C_{ox} and C_s for the capacitance of the oxide and that of the space charge layer, respectively. The emission rate from the trap is written as:

$$e_n = \nu \times \sigma_n \times N_c \times \exp\left(-\frac{\Delta E}{kT}\right), \tag{2}$$

where ν is the mean thermal velocity of electrons, σ_n is the capture cross section and N_c is the effective density of states in the conduction band. The DLTS response of the above mentioned structure was measured at sampling events chosen to fit the following scheme: t_1, $2t_1$ and $4t_1$. Sometimes, two sampling times, t_1 and t_2, are used, only at which $t_2 = 2 \times t_1$. The resulting correlated charge DLTS signal S_c is given by following equation:

$$S_c = Q(t_1) - 1.5Q(2t_1) + 0.5Q(4t_1). \tag{3}$$

3.2. Capacitance–voltage measurements (C–V)

Capacitance of the MOS diodes as a function of the gate bias was measured by the improved feedback charge measurements in the time domain. The feedback charge C–V method was described for the first time by Mego [27] and commercial Keithley stand-alone instrument is available. Originally, the latter has been intended for measurements of the steady-state (dc) time-domain capacitance of semiconductor devices. Bias step Δu_0 is applied to the unknown capacitance C of the investigated structure and consequently the change (time dependent) of output voltage Δu of the integrator is registered. The capacitance C is given by the relation $C = C_F(\Delta u/\Delta u_0)$, where $C_F = 3.3$ nF and $\Delta u_0 = 60$ mV are used in our experiments. The sampling time was set to 10 m s. C_Q–V measurements and Q-DLTS were carried out using the home-made spectrometer developed at the Institute of Physics of SAS Bratislava, Slovakia [22].