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Short Communication

Measurement of the quantum capacitance from two-dimensional surface state of a topological insulator at room temperature

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ABSTRACT

A topological insulator (TI) is a new kind of material that exhibits unique electronic properties owing to its topological surface state (TSS). Previous studies focused on the transport properties of the TSS, since it can be used as the active channel layer in metal-oxide-semiconductor field-effect transistors (MOSFETs). However, a TI with a negative quantum capacitance (QC) effect can be used in the gate stack of MOSFETs, thereby facilitating the creation of ultra-low power electronics. Therefore, it is important to study the physics behind the QC in TIs in the absence of any external magnetic field, at room temperature. We fabricated a simple capacitor structure using a TI (TI-capacitor: Au-TI-SiO_2-Si), which shows clear evidence of QC at room temperature. In the capacitance-voltage (C-V) measurement, the total capacitance of the TI-capacitor increases in the accumulation regime, since QC is the dominant capacitive component in the series capacitor model (i.e., $C_T^{-1} = C_Q^{-1} + C_{SiO2}^{-1}$). Based on the QC model of the two-dimensional electron systems, we quantitatively calculated the QC, and observed that the simulated C-V curve theoretically supports the conclusion that the QC of the TI-capacitor is originated from electron–electron interaction in the two-dimensional surface state of the TI.

1. Introduction

Recently, topological insulators (TIs) have received increasing attention due to their unprecedented unique quantum properties, i.e., the surface of a TI is metallic, but its bulk is insulating. This physical property is due to surface states of the material. Conventionally, many studies have tried to reveal these effects through carrier transport measurements. However, it is not trivial to identify the channel or the region in the TI material that contributes the most to the experimental results caused by carrier transportation. Among the four conduction channels that were reported to exist in the three-dimensional TI [1], it was found that each channel physically originated from the topological surface state, bulk carriers, impurity bands (IBs), and two-dimensional states on its sub-surface of the material. A few studies suggested new techniques to avoid the interference in bulk by engineering the mole fraction of the TI material [2] or by impurities doping in the TI material [3]. A method for measuring the quantum capacitance (QC) of the TI material has been proposed to eliminate the bulk interference completely [4]. This method directly measures the two-dimensional surface state leading to QC.

Recently, a TI has been considered as a material for future complementary metal-oxide-semiconductor (CMOS) devices [4]. Previous works [4,5] have investigated the physical properties of the TI material at low temperature such as 4 K and 77 K. However, it is very important to investigate the physical properties of the TI material at room temperature for CMOS applications. One of the physical properties of the TI material is the negative QC, and it can be very useful for the implementation of low power negative capacitance CMOS devices [6]. To adopt the TI material for future CMOS devices, it is critical to understand and quantify physically the QC of TIs at room temperature. It is known that, when one of the metal electrodes in a metal-insulator-metal (MIM) capacitor has a low density-of-system (DOS), the effect of QC is revealed. At the interface between Bi_2Te_3 (a TI material used in this study) and SiO_2, two-dimensional surface state can be formed when the quantum confinement effect works adequately. In this study, a topological insulator capacitor [TI-capacitor: Au (top electrode) – TI (insulator) – SiO_2 (insulator) – Si (bottom electrode)] is proposed and fabricated. By measuring the capacitance-voltage (C-V) of the TI-capacitor at room temperature, it was observed that the total capacitance of the TI-capacitor monotonically increases in

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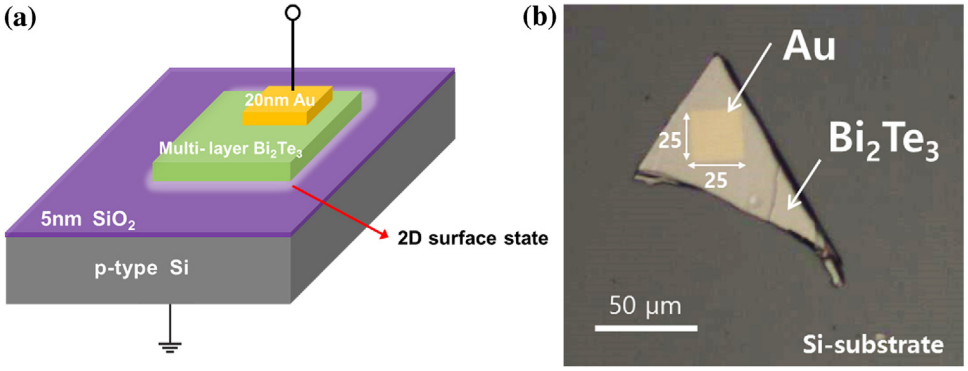

Fig. 1. (a) Illustrated bird's-eye view and (b) optical microscope image of a topological insulator (TI) capacitor. Bi_2Te_3 flakes are placed on the SiO_2 layer of the Si substrate using the mechanical exfoliation method.

accumulation mode. This explicitly indicates that the enhanced total capacitance is due to the QC in the TI material.

2. Materials and methods

The atomic structure of Bi_2Te_3 has the stacked interlayers forming quintuple layers [7]. The van der Waals force exists between the quintuple layers, so that it is much weaker than the adhesion force between Bi_2Te_3 and SiO_2. Therefore, Bi_2Te_3 flake can be easily transferred onto the SiO_2/Si substrate using "graphene-like" mechanical exfoliation method [8].

To fabricate TI-capacitor, firstly, a silicon substrate with a 5-nm-thick SiO_2 layer was cleaned using the standard cleaning procedure with methanol, acetone, and de-ionized (DI) water. Cleaved flakes of bulk Bi_2Te_3 were placed on the SiO_2 layer of the silicon substrate in air. The transmission electron microscope (TEM) image clearly shows the thickness of the Bi_2Te_3 flake (i.e. 760 nm) and the interface condition between Bi_2Te_3 and SiO_2, which are shown in Fig. 2(a) and (b), respectively. Then the square-patterned (25 μm × 25 μm) top gate, made of gold, in the TI-capacitor was fabricated using conventional photolithography and thermal evaporation. The TI-capacitor structure and optical microscope images are shown in Fig. 1(a) and (b), respectively. In order to measure the intrinsic capacitance of the TI-capacitor without any parasitic capacitance, the top electrode of gold is formed on the Bi_2Te_3 flake [see Fig. 1(b)].

3. Results and discussion

The other parasitic capacitances in the TI-capacitor are eliminated to detect the QC in the C-V measurement. All the possible capacitive components of the TI-capacitor are summarized in Fig. 3(a). C_B and C_Q denote the bulk capacitance and the QC of Bi_2Te_3, respectively. C_{SiO2} is the geometric capacitance of the oxide layer. The silicon substrate has its own capacitance (C_{Si}), which is varied depending on the operating modes of the capacitor, i.e., accumulation and depletion modes. For theoretical reasons, the bulk capacitance (C_B) can be neglected. First, when a high frequency ac signal (i.e., $f > 1$ kHz) is applied to the TI-capacitor, the carriers in the bulk of the TI material cannot respond to the applied ac signal [4]. Second, the bulk of the TI material has its own conductivity. Since the TI material, such as Bi_2Te_3, is very sensitive to the environment around it, the Te atoms in the bulk diffuse out and leave vacancies behind when the Bi_2Te_3 flake is exposed to air. These defects cause impurity states in the bandgap, which is called the IB, leading to the conductivity in the bulk of the TI material [9]. Considering the aforementioned physics, the capacitive model is revised from the one shown in Fig. 3(a) to that in Fig. 3(b). $C_{A/D}$ denotes the accumulation or depletion capacitance of the silicon substrates, which is varied as a function of the gate voltage. Note that C_A means the capacitance resulted from the Debye length at the surface of the silicon substrate (C_A is normally much larger than the other capacitances) [10]. Therefore, C_A can be considered negligible in the accumulation mode. In contrast, the depletion capacitance

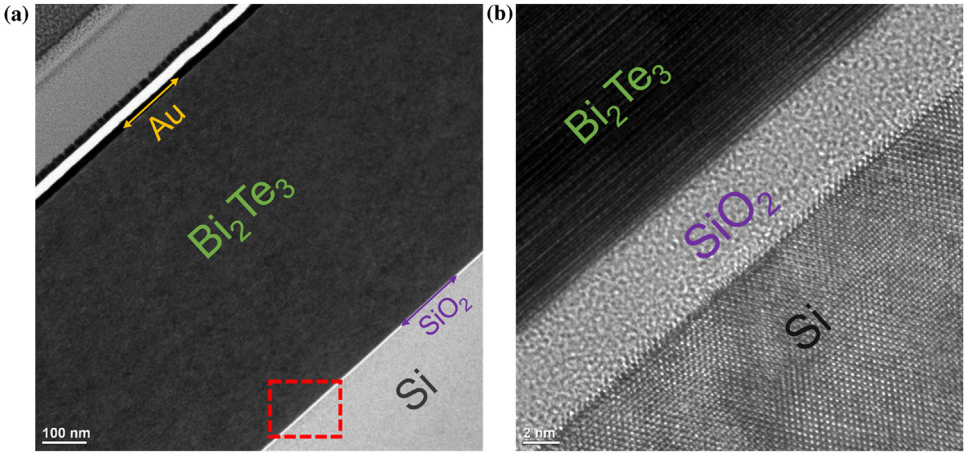

Fig. 2. Transmission electron microscope (TEM) image of TI-capacitor. (a) It shows all different thicknesses of each layer in the TI-capacitor (i.e. the thickness of Au, Bi_2Te_3 and SiO_2 are 20 nm, 760 nm and 5 nm, respectively). The specific interface condition between Bi_2Te_3 and SiO_2 can be observed in the red dashed box. (b) The high resolution TEM image confirms the clean interface quality between Bi_2Te_3 and SiO_2. The layered structure of Bi_2Te_3 is also shown in this high magnification image. (For interpretation of the references to colour in this figure legend, the reader is referred to the web version of this article.)