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Full Length Article

Influence of oxidation temperature on the interfacial properties of n-type 4H-SiC MOS capacitors

Yifan Jia[a], Hongliang Lv[a], Qingwen Song[a,b,*], Xiaoyan Tang[a,**], Li Xiao[c], Liangyong Wang[c], Guangming Tang[c], Yimen Zhang[a], Yuming Zhang[a]

[a] School of Microelectronics, Xidian University, Key Laboratory of Wide Band Gap Semiconductor Materials and Devices, Xi'an 710071, China
[b] School of Advanced Materials and Nanotechnology, Xidian University, Xi'an 710071, China
[c] Zhongxing Telecommunication Equipment Corporation, Shenzhen 518057, China

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ABSTRACT

The effect of oxidation temperature on interfacial properties of *n*-type 4H-SiC metal-oxide-semiconductor capacitors has been systematically investigated. Thermal dry oxidation process with three different oxidation temperatures 1200 °C, 1300 °C and 1350 °C were employed to grow SiO_2 dielectric, following by the standard post-oxidation annealing (POA) in NO ambience at 1175 °C for 2 h. The root mean square (RMS) roughness measured by Atomic Force Microscopy for the thermally grown SiO_2 before POA process is reduced with increasing the oxidation temperature, obtaining an atomically flat surface with a RMS of 0.157 nm from the sample oxidized at 1350 °C. Several kinds of electrical measurements were used to evaluate the densities of near interface traps and effective fixed dielectric charge for the samples, exhibiting a trend reduced with increasing the oxidation temperature. The interface state density of 3×10^{11} $cm^{-2}eV^{-1}$ at 0.2 eV from the conduction band edge was achieved from conductance method measurement for the sample oxidized at 1350 °C. The results from Secondary Ion Mass Spectroscopy and X-ray Photoelectron Spectroscopy demonstrate that high oxidation temperature can reduce the width of transition layer, the excess Si and silicon suboxide compositions near the interface, leading to effective improvement of the interfacial properties.

1. Introduction

Silicon carbide (SiC) metal-oxide-semiconductor field-effect transistors (MOSFETs) are expected to replace Si-based MOSFETs for high-temperature and high-power applications, owing to its superior material properties such as high critical breakdown electric field strength, high electron saturation velocity and high thermal conductivity. Besides its excellent properties, only stable silicon dioxide (SiO_2) insulator on SiC can be grown by conventional thermal oxidation process, which makes fabricate SiC metal-oxide-semiconductor (MOS) devices far more easily compared with the other wide band gap semiconductors.

Although the 4H-SiC MOSFETs are already commercial available for a few years, the SiO_2/SiC interface quality and oxide reliability are still the key issues limiting the development of the high performance 4H-SiC MOSFETs [1–4]. Such high density of charge traps near the interface seriously degrade the channel mobility of the SiC MOSFET, resulting in a higher on-resistance and the threshold-voltage instability and restricting the wide band gap advantage of 4H-SiC [1,2]. The previous researches mainly focused on the effect of the different POA processes on improvements of SiO_2/SiC interface system, such as POA in nitrogen or phosphorus containing ambulance, and showed that the nitrogen and phosphorus based annealing can effectively improve the interface quality [5–8]. However, in addition to the POA treatment process, the impact of the oxidation temperature on the SiO_2/SiC interface quality is also required to further research. The previous thermal oxidation processes for 4H-SiC were typically performed at the maximum operating temperature of 1200 °C in the common quartz furnace, so the oxidation at higher than 1200 °C becomes attractive. Recent reports on the high-temperature oxidations (>1200 °C) of 4H-SiC have shown that the density of interface states (D_{it}) can be decreased [9–14]. The influence of the thermal oxidation

* Corresponding author at: School of of Advanced Materials and Nanotechnology, Xidian University, Xi'an 710071, China.
** Corresponding author at: School of Microelectronics, Xidian University, Xi'an 710071, China.
E-mail addresses: qwsong@xidian.edu.cn (Q. Song), xytang@xidian.edu.cn (X. Tang).

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Table 1
Thermal processing steps used for each of the samples.

Samples	Thermal oxidation	NO annealing
1200 °C	@1200 °C (180 min)	@1175 °C (120 min)
1300 °C	@1300 °C (30 min)	@1175 °C (120 min)
1350 °C	@1350 °C (15 min)	@1175 °C (120 min)

temperature on D_{it} was reported in 2006 by Kurimoto et al. [9]. The work reported by Kikuchi et al. showed a very low D_{it} in a 14 nm oxide thickness sample by thermal oxidation at 1300 °C with O_2 annealing, in which the temperature window for the ideal reaction of SiC thermal oxidation in O_2 ambience with a standard atmospheric pressure was approximately estimated to be 1100–1400 °C [10,11]. Recently, higher oxidation temperature up to 1400 °C was also used to form the SiO_2 reported by Naik et al. [12], however the results processed in 1400 °C were not as good as the expectation of better mobility at such higher oxidation temperature, and a channel mobility of corresponding MOSFETs was only 2 cm^2/Vs. In this case, Ref. [15] reported that the oxidation process with higher than 1400 °C enhances interstitial C injecting into SiC, resulting in large amounts of scattering centers as well as traps in the SiC inversion channel. Although great effort has been made on SiC high temperature oxidation and a number of studies on the effect of the oxidation temperature on the density of interface states has been reported, these is not enough information about the influence of the high oxidation temperature on near interface traps (NITs) and effective fixed dielectric charge (N_{eff}). Recent works have shown the existence of a kind of NITs in the SiC MOS devices, which can exchange charge with the semiconductor easily and could significantly affect the channel mobility [16,17]. However, the relationship of NITs with the oxidation temperature in the 4H-SiC MOS devices is still not very clear. Therefore, the further investigation is required for the mechanism of oxidation temperature influence on the NITs and N_{eff} of 4H-SiC MOS devices.

In this paper, three different high oxidation temperatures 1200 °C, 1300 °C and 1350 °C were employed to grow SiO_2 dielectric on n-type 4H-SiC to figure out the effects of high oxidation temperature on the SiO_2/SiC interface characteristics and quality of SiO_2 film, and the improvement mechanism of interfacial characteristics is further investigated by Atomic Force Microscopy (AFM), capacitance-voltage (C-V), conductance-frequency (G-f), current-voltage (I–V), Secondary Ion Mass Spectroscopy (SIMS) and X-ray Photoelectron Spectroscopy (XPS) measurements.

2. Experimental methods

4H-SiC wafer with an epitaxial layer thickness of 13 μm and nitrogen-doped concentration of 7.8×10^{15} cm^{-3}, grown on silicon faced 4° off-axis *n*-type substrate purchased from EpiWorld International Co., Ltd., was used in this experiment. Following the RCA cleaning, a HF dip and water rinsing, thermal oxidation was carried out in dry O_2 environment at temperatures of 1200 °C (180 min), 1300 °C (30 min) and 1350 °C (15 min), respectively. The surface morphological properties of thermally grown SiO_2 were assessed by Keysight 5500 Atomic Force Microscopy after the high-temperature oxidation processes. Besides, the C-V characteristics before POA were measured by Hg probe test platform in clean room using the duplicate samples, which were cut from the same wafer and oxidized in the same furnace. Afterwards, all of the samples without Hg probe test were annealed using the conventional NO annealing process (1175 °C for 2 h). The thermal processing steps are summarized for all samples in Table 1. The oxide thicknesses (d_{ox}) measured by J.A.Woollam M2000D sepctroscopy ellipsometry (SE) were 49 nm, 51 nm and 57 nm for the samples oxidized at 1200 °C, 1300 °C and 1350 °C, respectively. Finally, MOS capacitor structure was fabricated, Ni was evaporated for the backside ohmic contact and Al was sputtered on the oxide surface to form the gate electrode.

Electrical characteristics of the samples in this study were measured on a CASCADE probe station, using a Keysight B1505A Semiconductor Parameter Analyzer. The SiO_2/SiC interface characteristics were evaluated by high frequency bidirectional capacitance-voltage and accumulation conductance–frequency measurements. The densities of near interface traps were extracted from the hysteresis of the bidirectional C-V curves and the densities of interface states were determined by the conductance method. Gate oxide integrity (GOI) was evaluated by I-V measurements, and the forward I-V measurements were performed at room temperature by sweeping the leakage current up to 100 nA. The density of incorporated nitrogen and the relative contents of Si, O and C in the samples were determined by SIMS measurements in Evans Analytical Group (EAG) laboratories, and the width of the transition layer was extracted from the SIMS profile. The chemical bonding states at the interface were examined via Thermo Scientific X-ray Photoelectron Spectroscopy, in which a monochromatic Al Kα X-ray excitation ($h\upsilon$ = 1486.68 eV) was used at a takeoff angle of 90° on the different samples. Argon ion sputtering was carried out in the same ultrahigh-vacuum chamber to remove the SiO_2 layer gradually.

3. Results and discussion

3.1. Surface morphology

Firstly, the surface morphology of the 4H-SiC epitaxial layer before oxidation process and the SiO_2 prepared with different oxidation temperatures were examined by AFM with testing area of 5×5 μm^2 and 10×10 μm^2. It is found that the statistical value of RMS and the maximum roughness for a given sample with different scan area are similar, so for the testing with better resolution, the typical results from testing area of 5×5 μm^2 are shown in Fig. 1. A smooth morphology (RMS = 0.139 nm) was observed on the SiC epitaxial surface before oxidation process (Fig. 1(a)), in which the maximum roughness is below 1.3 nm. Comparing with the 4H-SiC epitaxial layer, the values of surface RMS for the three grown SiO_2 samples become larger. Besides, it is found that there are some protuberances with the peak height about 3.7 nm on the surface of the three oxidized samples. Moreover, the numbers of the protuberances are gradually reduced with increasing oxidation temperature. The surface morphological images exhibit that the value of RMS is related with the protuberances. Under 1200 °C oxidation condition (Fig. 1(b)), the RMS roughness is 0.379 nm and large numbers of the protuberances are observed. The sample oxidized at 1300 °C (Fig. 1(c)) shows a RMS roughness of 0.231 nm with several isolated surface protuberances. In the case oxidized at 1350 °C, as shown in Fig. 1(d), there is only one obvious protuberance observed at the edge of the 5×5 μm^2 testing area. Thus, it is found that an atomically flat surface with a RMS roughness of only 0.157 nm is achieved and protuberances are almost successfully eliminated by high temperature oxidation process at 1350 °C. It is inferred that the surface protuberances may be related to the lattice mismatch of some incompletely reacted atoms and the higher oxidation temperature may help to restrain the formation of this kind of protuberances. In addition, it is worth noting that the peak heights of the protuberances for all of the samples are reduced into less than 2 nm after POA in NO ambience (not shown here). It is suggested that the NO POA induces a slow re-oxidation process and high-temperature condition may help the surface atoms to be redistributed, thus improving the surface morphology compared with the original thermal oxidation.