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Impact of Gd_2O_3 passivation layer on interfacial and electrical properties of atomic-layer-deposited ZrO_2 gate dielectric on GaAs

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ZrO_2 gate dielectric films were fabricated on n-GaAs substrates by atomic layer deposition (ALD), using metal organic chemical vapor deposition (MOCVD)-derived ultrathin Gd_2O_3 film as interfacial control layer between ZrO_2 and n-GaAs. The interfacial structure, capacitance–voltage and current–voltage properties of ZrO_2/n-GaAs and ZrO_2/Gd_2O_3/n-GaAs metal-oxide-semiconductor (MOS) capacitors have been investigated. The introduction of an ultrathin Gd_2O_3 control layer can effectively suppress the formation of As oxides and high valence Ga oxide at the high *k*/GaAs interface which evidently improved the electrical properties of GaAs-based MOS capacitors, such as higher accumulation capacitance and lower leakage current density. It was found that the current conduction mechanism of MOS capacitors varied from Poole–Frenkel emission to Schottky–Richardson emission after introducing the thin Gd_2O_3 layer. The band alignments of interfaces for ZrO_2/GaAs and ZrO_2/Gd_2O_3/GaAs were established, which indicates that the conduction band offset (CBO) for ZrO_2/GaAs and ZrO_2/Gd_2O_3/GaAs stacks are ~1.45 and ~1.62 eV, correspondingly.

1. Introduction

In the recent years, along with developing of the scaling of microelectronics devices, GaAs semiconductor has been attracting vast interests as a candidate for metal-oxide-semiconductor field effect transistor (MOSFET) owing to its relatively high effective channel mobility [1–7]. However, the fabrication of GaAs transistors remains a striking challenge due to a poor GaAs/oxide interface which is easy to lead to the Fermi-level pinning and degraded electrical properties [8–12]. Recently, the high-*k* materials are proposed as the gate dielectrics for GaAs-based MOSFET applications [1–4]. Furthermore, ZrO_2 is considered to be a promising candidate gate dielectric in GaAs-based MOSFET due to a relatively high dielectric constant (*k*) and a wide energy band gap. Unfortunately, the direct deposition of ZrO_2 on GaAs has shown a poor interface, which results in high density of interface traps [13,14]. Some reports have shown that Gd_2O_3 seems to be one of the most attractive candidates for the oxide/GaAs interface passivation [15,16]. However, the effect of Gd_2O_3 layer on the band alignments, interfacial and electrical properties of atomic-layer-deposited ZrO_2 on GaAs is unknown. Here, we fabricate ZrO_2 gate dielectric films on n-GaAs substrates by atomic layer deposition (ALD) method, using metal organic chemical vapor deposition (MOCVD)-derived ultrathin Gd_2O_3 film as interfacial control layer between ZrO_2 and n-GaAs. The interfacial structure, the band alignments, capacitance–voltage and current–voltage properties of ZrO_2/n-GaAs and ZrO_2/Gd_2O_3/n-GaAs metal-oxide-semiconductor (MOS) capacitors have been investigated comparatively. We find that the incorporation of an ultrathin Gd_2O_3 interfacial control layer has proved that it can significantly improve the electrical properties of GaAs-based MOS capacitors.

2. Experiment

Si-doped n-type GaAs (1 0 0) wafers with a doping concentration of $2.4 \times 10^{18}\ cm^{-3}$ were used as the substrates. The cleaning method and chemical treatment of GaAs wafers were described in Ref. [17]. Briefly, the wafers were degreased in acetone, ethanol and isopropanol for 10 min, respectively. Then the wafers was immersed in a 1:3 solution of HCl:H_2O for 3 min to remove the surface nativeoxide layer. Finally, S passivation of the wafers was done in a diluted $(NH_4)_2S$ aqueous solution at room temperature for 30 min. In order to eliminate the effect of air exposure time, the S-passivated samples were immediately transferred into the reaction chamber of metal organic chemical vapor deposition (MOCVD) for Gd_2O_3 deposition. And ultrathin layers of Gd_2O_3 were deposited at 500 °C for 2 min using $Gd(DPM)_3$ [DPM = tris(2,2,6,6-tetramethyl-3-5-heptanedionato)] as MOCVD precursor. The thickness of Gd_2O_3

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ultrathin layer of ∼1 nm was estimated based on the deposition rate of MOCVD and the Ar ion sputtering rate in the XPS depth profiles of Fig. 1(a). At the same time, the S-passivated control samples without Gd_2O_3 layer were under way. After Gd_2O_3 deposition, the samples with and without Gd_2O_3 layer were simultaneously placed into an ALD reactor (Picosun SUNALE^{TM} R-150B) for the ZrO_2 films deposition at 300 °C. The air exposure time of the samples with and without Gd_2O_3 are almost the same between $(NH_4)_2S$ passivation and ALD. $ZrCl_4$ and H_2O were used as the ALD sources. The pulse of the ALD sources was 0.1Ys and N_2 purge pulse of 6Ys was used to remove redundant reactants and gaseous reaction byproducts. The ∼5Ynm-thick ZrO_2 films were fabricated on two kinds of GaAs with and without Gd_2O_3 layers, respectively. Subsequently, all samples were annealed at 500 °C for 30Ys in nitrogen atmosphere by rapid thermal annealing. Then MOS structure was fabricated by sputtering Pt top electrode with diameter of 200 μm through shadow masks. The back contact was formed by pasting silver paint (SPI-CHEM) on fresh GaAs surface scraped by diamond cutting tool. Another set of samples with ∼1 nm ZrO_2 films were also prepared using same process in order to characterize the interfacial chemical structure between dielectrics and substrates by X-ray photoelectron spectroscopy (XPS, Thermo K-Alpha) with a monochromatic Al *Kα* source ($h\nu$ = 1486.6 eV). The valence band (VB) and the band gap were determined by XPS valence band spectra and O 1s energy loss spectroscopy with a monochromatic Al *Kα* source (1486.6 eV) source and a pass energy of 20 eV (using a Thermo ESCALAB 250), respectively.

3. Results and discussion

Fig. 1(a) shows the Gd 3d XPS depth profiles of sample with Gd_2O_3 interfacial control layer between ZrO_2 and n-GaAs. The energy and etching time of Ar ion sputtering between each XPS spectrum were 1000 eV and 15Ys, respectively. The Gd oxide signals were obtained after sputtering 30Ys, indicating the formation of thin Gd_2O_3 interface layer between ZrO_2 and GaAs. The As 3d and Ga 2p spectra at the interface of ZrO_2/GaAs and ZrO_2/Gd_2O_3/GaAs samples are shown in Fig. 1(b) and (c), respectively. For the ZrO_2/GaAs sample, the peak with binding energy at 44.3 eV attributes to the As—O bonds. While at the same position, the As—O peak is not observed for the ZrO_2/Gd_2O_3/GaAs sample. In Fig. 1(c), for the direct deposition of ZrO_2 sample on GaAs, the Ga 2p3/2 spectra at ZrO_2/GaAs interface clearly shows the presence of high valence oxides (GaO_x), implying that the Ga—O peak may shift to higher oxidation states. These results from Fig. 1(b) and (c) indicate that the introduction of thin Gd_2O_3 control layer can effectively suppress the formation of As oxides and high valence GaO_x at the high *k*/GaAs interface. The disappearance of As oxides

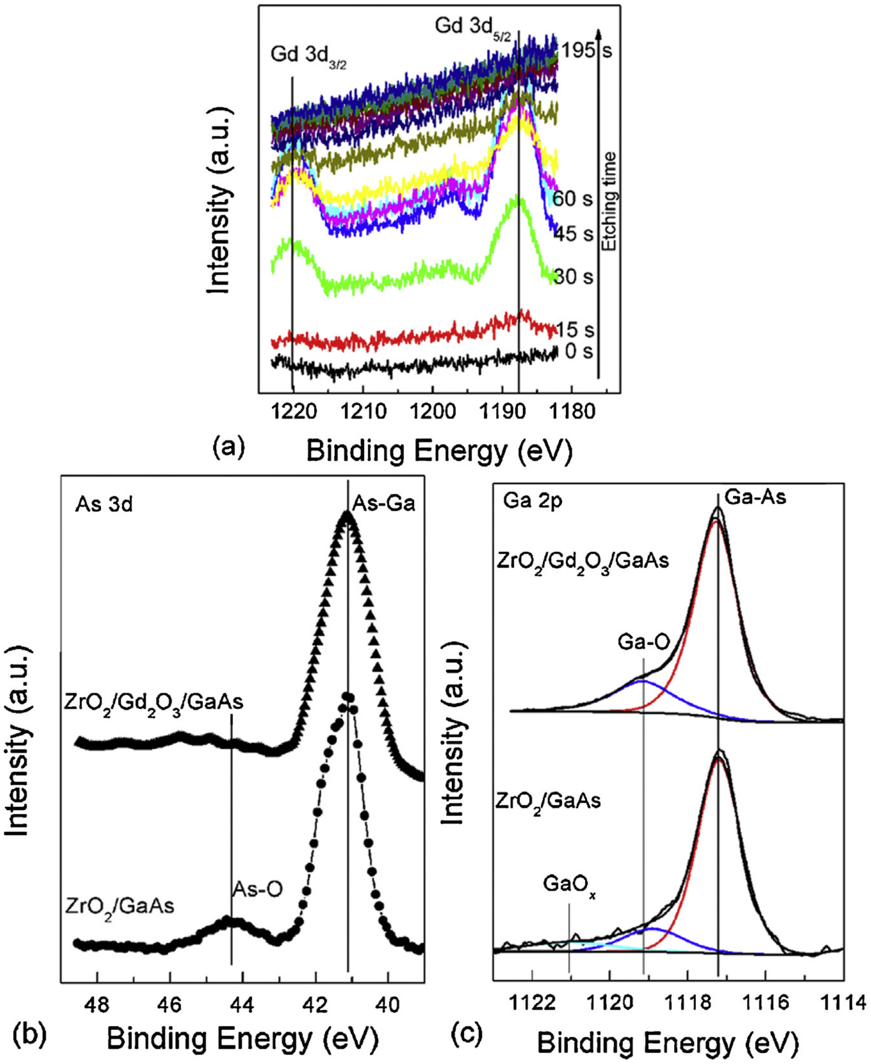

Fig. 1. (a) Gd 3d XPS depth profiles of sample with Gd_2O_3 interfacial control layer between ZrO_2 and GaAs. (b) As 3d and (c) Ga 2p3/2 spectra of ZrO_2 on GaAs with and without Gd_2O_3 control layers.