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# Control of the graphene growth rate on capped SiC surface under strong Si confinement

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ABSTRACT

The effect of the degree of Si confinement on the thickness and morphology of UHV grown epitaxial graphene on (000−1) SiC is investigated by using atomic force microscopy and Raman spectroscopy measurements. Prior to the graphene growth process, the C-face surface of a SiC substrate is capped by another SiC comprising three cavities on its Si-rich surface with depths varying from 0.5 to 2 microns. The Si atoms, thermally decomposed from the sample surface during high temperature annealing of the $SiC_{cap}/SiC_{sample}$ stack, are separately trapped inside these individual cavities at the sample/cap interface. Our analyses show that the growth rate linearly increases with the cavity height. It was also found that stronger Si confinement yields more uniform graphene layers.



## 1. Introduction

The epitaxial production of graphene in a controllable way has attracted a major interest since it offers a large scale template for carbon based two dimensional electronics [1–3]. The quality of graphene is largely governed by the production methods and the processes involved. The graphene layers can be prepared epitaxially on both Si-terminated (0001) and C-terminated (000−1) polar faces of a SiC crystal simply by surface thermal decomposition process. A number of different experiments have been conducted to produce graphene especially on the C-face surface of SiC due to the very tempting rotational stacking disorientation of the grown layers [4]. Due to this unique stacking structure, the layers forming the stack are electronically decoupled from each other and thus each layer exhibits Dirac-cone like band dispersion very similar to that of an isolated monolayer graphene [5]. Nevertheless, compared to the Si-face surface of SiC, the growth is much faster on the C-face due to high sublimation rate of Si atoms during the high temperature annealing process in vacuum [5,6]. Hence, for the same growth conditions, multiple layers are more readily formed on the C-face than on the Si-face surface of SiC. Another important aspect is that the elevated Si evaporation rate on C-face SiC leads to the formation of unavoidably high concentration of crystalline defects in the graphene matrix. In order to obtain defect free films with desired thickness uniformity on this particular polar surface, a precise control over the Si evaporation rate is necessarily required.

A variety of different approaches, based on the confinement controlled sublimation of Si, are employed to reduce the uncontrollable growth rate of epitaxial graphene on the C-face SiC. In order to maintain a decreased growth rate even at elevated temperatures (e.g., >1500 °C), a sufficient amount of Si vapor density must be maintained on the SiC surface. Currently, thin and homogeneous graphene layers have been prepared by high temperature annealing of the SiC crystals either in an inductively heated graphite enclosure placed inside a high vacuum furnace [3] or in an inert argon atmosphere [7,8]. The use of a Si containing environment such as disilane ($Si_2H_6$) was also found to yield improved graphene morphology with relatively large domain sizes [9]. We have recently showed that the confinement of sublimated Si atoms at the interface between a $SiC_{cap}/SiC_{sample}$ stack significantly reduces the graphene growth rate on the C-face SiC down to an easily controllable range even in ultra high vacuum (UHV) environment [10]. Despite those progresses, the control of the preparation conditions for epitaxial graphene is still under discussion and the employed growth methods require further research.

## 2. Experimental methods

We have systematically studied the effect of the degree of Si confinement on the thickness and morphology of epitaxial graphene prepared in UHV conditions. For this purpose, the C-face surface of a SiC sample was capped by another SiC substrate comprising

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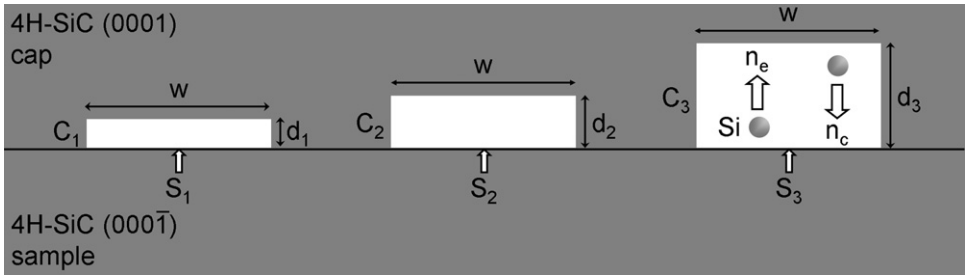


**Fig. 1.** Schematic illustration of the SiC–SiC capping comprising three individual cavities with different orifice heights of $d_1 = 0.5\ \mu m$, $d_2 = 1.0\ \mu m$, $d_3 = 2.0\ \mu m$.

equally spaced three cavities with different depths on its Si rich polar face. When placed on the sample surface, the cavities on the capping substrate provide well defined separations with the same sample surface area but different orifice heights between the cap and sample surfaces as seen in Fig. 1. During the high temperature annealing process (~1500 °C), the Si atoms evaporated from each capped region of the sample surface were trapped inside the corresponding cavity on top. The cavities between the cap and the sample surface create small volumes of Si vapor density varying with the amount of confinement in each cavity. The presence of Si vapor pressure acting on each capped region retard the sublimated Si atoms to escape freely into vacuum environment. The local confinement of Si vapor in these small volumes promotes the constituent Si atoms to condense back on to the sample surface and thus leads to such a low graphene growth rate that is dependent only on the cavity's orifice height. In this experiment the annealing temperature and the growth duration are inherently the same for all three growth surfaces. Therefore, the graphene thickness is essentially correlated only with the orifice height. This can be understood as in the following manner. Assume that the SiC sample is held in a hermetically sealed and nonreactive enclosure which is surrounded by vacuum at temperatures high enough to break the Si—C bond (e.g., >1100 °C) [11]. In this case, the Si atoms evaporated from the SiC surface are fully trapped inside this closed environment. In the thermodynamic equilibrium, since the evaporated Si atoms recombine on the SiC surface and the evaporation rate of Si ($n_e$) is balanced with its condensation rate ($n_c$) in the close vicinity of the sample surface, graphene does not form at any temperature. The graphene growth can be facilitated only if some of the vapor phase Si is released out of the confinement through a hole or an orifice created on the wall of the enclosure. The growth rate of graphene is then simply proportional to the Si release rate which can be tuned only by changing the dimensions of the leak area for the fixed temperature. Assuming a uniform velocity and density distribution of Si vapor inside the cavity, the growth rate under the influence of such a closed Si confined medium can be written as $n_g = ne - nc = N/S$, where $N = Av_a\rho$ is the release rate of Si through the leak area of $A$, $\rho$ is the Si vapor density acting on the sample surface of $S$ and $v_a = (8\,kT/\pi m)^{1/2}$ is the average thermal speed of the Si atoms with mass $m$ at temperature $T$ in the vapor [3,10].

In our experiments, we used 3 mm wide and 10 mm long n-type 4H—SiC substrates as the cap material. The cap has three equally spaced cavities with the same surface area, $S = 1.5\ mm \times 3\ mm$ but with different depths on its Si-terminated face. The cavities were fabricated by dry etching technique in three subsequent processes. The cavities labeled as $C_1$, $C_2$ and $C_3$ in Fig. 1(a) have the etch depths of $d_1 = 0.5\ \mu m$, $d_2 = 1.0\ \mu m$ and $d_3 = 2.0\ \mu m$, respectively as determined by a surface profiler with a height resolution better than 0.01 μm. After the chemical cleaning and oxide removal process in diluted HF acid, the capping substrate was then annealed by resistive heating at 1450 °C for 15 min in a UHV chamber with base pressure of $P < 1 \times 10^{-10}$ mbar. This annealing procedure does not only remove the possible traces of surface contamination and remaining surface oxide, but also creates a non-reactive thin graphitic layer over the cap surface. The presence of such a chemically inert and high temperature compatible graphitic layer at the interface between the SiC/SiC stack, prevents the fusion welding of the SiC cap with the underlying SiC substrate during the high temperature annealing process.

The pre-annealed cap was placed on top of a C-face SiC sample with the same dimensions and polytype as the capping substrate. The cavities on the capping substrate provide well defined gaps with rectangular orifices between its surface and the sample surface as illustrated in Fig. 1. The uniformity of the separations between the two semi-transparent SiC substrates was verified by optical microscopy and optical interference patterns. Following the thermal cleaning cycle as described in Ref. [10], the sample-cap stack was annealed in UHV for 20 min at 1500 °C for the graphene growth. The sample temperature was measured remotely by an optical pyrometer with 1 °C resolution. During the graphene growth stage the maximum chamber pressure was recorded as $2 \times 10^{-8}$ mbar. After splitting the stack, the regions on the sample surface, which were positioned underneath the cavities $C_1$,–$C_3$ during the annealing process, were characterized individually by atomic force microscopy (AFM) and Raman spectroscopy measurements.

## 3. Results and discussion

The surface morphology of our samples before and after the annealing process was investigated by AFM. The topography image shown in Fig. 2(a) is taken from the surface of as-received 4H—SiC, which is composed of about 0.5–0.6 μm wide atomically flat terraces due to ~0.1° miscut angle of the wafer surface. These well ordered arrays of the terraces are created during the preparation of the epi-ready wafer surface. After annealing the sample with the cap, we found that different morphologies were developed on the sample surface regions $S_1$, $S_2$ and $S_3$ positioned underneath the cavities $C_1$, $C_2$ and $C_3$ respectively. On the surface $S_1$, which had the highest confinement during the growth, a large number of well ordered and 1–4 μm wide stepped terraces were observed (Fig. 2(b)). Compared to the non-modified initial SiC surface, the height of the formed terraces is measured to be about 2 nm in average. Similar modification of the SiC surface has also been observed when the SiC crystals were annealed at high temperatures by other confinement controlled sublimation techniques [3,7]. Previous studies pointed out that the edges of these stepped terraces act as nucleation centers for the graphene formation [12,13]. The surface $S_2$, on which the growth is carried out under one half of the confinement of the $S_1$ surface, the surface morphology was found to be topographically rougher with a large number of travertine like flakes (Fig. 2(c)). The majority of these flakes spread over the terrace edges onto the neighboring terraces. Unlike $S_1$ and $S_2$, the surface morphology on $S_3$ reveals domain like features with distinct ridges. The presence of such flaky structures seen in Fig. 2(d) is associated with the growth of thicker graphene layers on the corresponding