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Charging behavior of silicon nitride based non-volatile memory structures with embedded semiconductor nanocrystals

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ABSTRACT

The charging behavior of MNS (metal-nitride-silicon) and MNOS (metal-nitride-oxide-silicon) structures containing Si or Ge nanocrystals were studied by capacitance–voltage (*C–V*) and memory window measurements and by simulation. Both the width of hysteresis of *C–V* characteristics and the injected charge exhibited exponential dependence on the charging voltage at moderate voltage values, while at high voltages the width of hysteresis of *C–V* characteristics and the injected charge exhibited saturation. The memory window for reference MNS structure without nanocrystals was wider than that for reference MNOS structures. The presence of nanocrystals enhanced the charging behavior of MNOS structures, but in MNS structures nanocrystals exhibited the opposite effect. The main conclusion is that the presence of nanocrystals or other deep levels close to the Si surface enhances the charge injection properties due to the increased tunneling probability, but nanocrystals or other deep levels located far from the Si surface in the nitride layer do not enhance, but even can degrade the charging behavior by the capture of charge carriers.

1. Introduction

The two basic types of memory elements used in non-volatile (EEPROM and flash) memories are the floating gate and the SONOS (silicon-oxide-nitride-oxide-silicon) field effect transistors (FETs). Floating gate memory arrays face difficulties with technology scale-down. The main problem is that the whole amount of stored charge carrying the information can be lost through defects or weak points of tunnel oxide with reduced thickness. One of the possible solutions is to replace the floating gate with separated semiconductor nanocrystals (NCs), which are electrically isolated [1].

But, in SONOS and MNOS (metal-nitride-oxide-silicon) devices (the latter were the first realized memory structures [2]) the charge is stored in traps located in the Si_3N_4 layer close to the Si_3N_4/SiO_2 interface. In these structures traps are isolated a priori. However, formation of semiconductor NCs in silicon nitride based structures can enhance their charging and/or retention behavior, as it was first demonstrated by Rao et al. for SONOS structures [3]. Nevertheless, only very few works are devoted to silicon nitride based memory structures with embedded NCs, even it seems obvious to merge the advantages of nanocrystal and silicon nitride based memory devices.

We have studied both MNS (metal-nitride-silicon) and MNOS structures with Si NCs, and compared their memory behavior to similar reference memory structures without NCs. MNOS structures with embedded Ge NCs have also been studied. For proper locations of NCs in MNOS structures enhanced charge injection and retention properties were obtained [4,5]. Some unexpected phenomena were also obtained in these structures. For example, in the case of MNS structures the effect of NCs on charge injection properties was opposite, that expected: the memory window shrinked with increasing duration of NC deposition [4,5].

In this paper some features of the charging behavior of the studied structures are discussed in terms of results of computer simulations performed for understanding the origin of these peculiarities. The electron and hole tunneling probabilities to the nanocrystals and to the nitride conduction/valence band were calculated for MNOS structures with and without nanocrystals using WKB approximation. Using these probabilities actual memory hysteresis characteristics were simulated to understand the effect of layer thicknesses and of the presence and location of nanocrystals.

2. Experiments and calculations

MNOS structures containing Si or Ge NCs at the Si_3N_4 interface were prepared, while MNS structures were prepared with Si

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NCs only. The SiO_2 tunnel layer was prepared after cleaning the (0 0 1) oriented n-type Si substrates in 1 wt% HF in both type of structures with Si or Ge NCs. The SiO_2 layer was prepared using a HNO_3 treatment [6]. The n-type Si wafers were immersed in 68 wt% HNO_3 at the boiling temperature (121 °C) for 60 min. This method yielded a SiO_2 layer with a thickness of 2.5 nm, as obtained by cross-sectional transmission electron microscopy (XTEM) [1]. For a part of MNOS structures with Ge NCs the tunnel oxide was prepared by a $H_2SO_4 + H_2O_2$ treatment [4,5].

The Si NC layer and the Si_3N_4 control layer were deposited by LPCVD at 830 °C at a pressure of 30 Pa using SiH_2Cl_2 and NH_3. The Si_3N_4 layers were grown at gas flow rates of SiH_2Cl_2 and NH_3 of 21 and 90 sccm, respectively, while for Si NC layer a gas flow rate of SiH_2Cl_2 of 100 sccm was used. The duration of deposition for the Si NC layer was 30 or 60 s (Sample Nos. COA030 and COA060, respectively). Reference structures without Si NC layer were also prepared (Sample No. COA000). The duration of deposition for the Si_3N_4 control layer was 15 min, which yielded a layer thickness of about 40 nm, obtained by XTEM and spectroscopic ellipsometry [1].

Ge NCs were deposited by electron gun evaporation at a pressure of 1×10^{-7} Torr [7]. During evaporation, and for an additional 1 min after this process, the substrate temperature was kept at 350 °C. The duration of evaporation was 25 and 50 s. After cooling down, the wafers were covered with LPCVD Si_3N_4 control layer at similar conditions, as in the case of structures with Si NCs, given above. Reference structures without Ge NCs were also prepared.

In the case of MNS structures prepared in similar way the effect of the deposition time of the middle Si NC layer was studied as well (30 s and 60 s – Samples NI030 and NI060, respectively). A reference structure without NCs was also prepared with a Si_3N_4 layer thickness of 40 nm (Sample NI000).

For electrical and memory measurements Al capacitors were formed with dimensions of 0.8 mm by 0.8 mm by evaporation. The charge injection properties were studied on the prepared capacitors by capacitance–voltage (*C–V*) and memory window measurements. To enhance the development of inversion layer, and so to avoid high voltage drop on the deep depletion layer during negative voltage pulses, the structures were illuminated with white light during memory window measurements. 8–12 capacitors were studied for each structure. The scatter of electrical and memory window parameters was less than 10% in each studied structure.

The tunneling probability of electrons and holes to nanocrystals and to the conduction or valence band of the nitride layer, respectively, has been calculated on the basis of WKB approximation [8]. The tunneling probabilities have been studied as a function of the electric field in the oxide layer, of the oxide thickness and of the size and location of nanocrystals [9] by using the band structure and band discontinuity data presented in Ref. [8].

Memory hysteresis curves were simulated by calculating the flat-band voltage shift due to the charge injected and stored in nanocrystals or in traps in the nitride layer. The net charge captured in nanocrystals or in the nitride layer during a voltage pulse, can be calculated by the integration of the difference of the current flowing into the structure via the oxide layer and that of flowing out of the structure via the nitride layer. The current via the oxide layer was obtained also by WKB approximation [8], while for current via the nitride our experimental results were used [10]. The details of integration is described elsewhere [11,12].

3. Results and discussion

3.1. Results of simulations

Fig. 1 presents the two extremes of electron tunneling probability to MNOS structures with or without embedded semiconductor nanocrystals as a function of the oxide thickness and the electric field in the oxide layer. One of these extremes is the tunneling probability to the conduction band of the nitride layer for MNOS structures with nanocrystals, if they are located deep in the nitride layer (deeper than the tunneling length shown in Fig. 2). This is the electron tunneling probability for MNOS structures without nanocrystals either. If NCs are located deeper, than the tunneling length, they do not influence the tunneling process directly. The other extreme is the tunneling probability to the nanocrystals located at the SiO_2/Si_3N_4 interface. It is just the tunneling probability via the oxide layer (resonant tunneling is not considered). The tunneling probability via NCs or traps [13] located deeper, but within the tunneling depth, is between these two extremes.

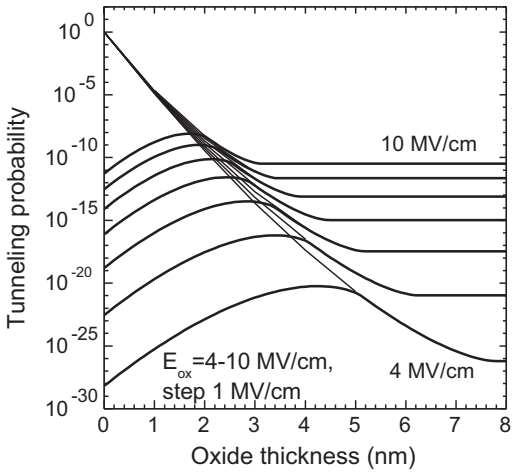

Fig. 1. The two extremes of electron tunneling probability to MNOS structures with or without embedded semiconductor nanocrystals as a function of the oxide thickness and the electric field in the oxide layer. Thick lines represent the tunneling probability to the conduction band of the nitride layer for MNOS structures with nanocrystals, if they are located deep in the nitride layer (deeper than the tunneling length – see Fig. 2), and for MNOS structures without nanocrystals. Thin lines represent the tunneling probability to the nanocrystals located at the SiO_2/Si_3N_4 interface (tunneling probability via the oxide layer).

The tunneling probability to the conductance band is higher for higher electric fields. It exhibits maximum as a function of oxide thickness, which depends on the actual electric field. The higher the electric field the thinner the oxide layer for the maximum probability. The increase of tunneling probability in the presence of a thin oxide layer in comparison with MNS structures without oxide layer, is due to a high potential drop on the oxide layer caused by its lower dielectric constant: the area of potential barrier above the electron energy is smaller, as it can be deduced from Fig. 2a [14]. At higher oxide thicknesses and/or electric fields the charge injection mechanism changes to direct tunneling to the nitride conductance band via the oxide layer, as shown in Fig. 2b. In this case the tunneling probability decreases with the further increase of oxide thickness. At high oxide thickness the tunneling probability saturates at a certain level. At this point the potential drop on the oxide layer just equals the barrier height at the SiO_2/Si_3N_4 interface, and the current mechanism changes to the Fowler–Nordheim tunneling of electrons to the oxide conduction band, as presented in Fig. 2c. For this injection mechanism the oxide thickness does not influence the tunneling probability [9].

The tunneling probability via the oxide layer (direct tunneling to NCS located at the SiO_2/Si_3N_4 interface) does not depend strongly on the electric field, but exhibits fast decrease with increasing the oxide thickness. For a given oxide thickness the two extremes merge at a certain electric field, when the modified Fowler–Nordheim tunneling to the nitride conductance band via the oxide and nitride layer (Fig. 2a) changes to direct tunneling via