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Influence of deposition conditions on electrical and mechanical properties of Sm_2O_3-doped CeO_2 thin films prepared by EB-PVD (+IBAD) methods. Part 1: Effective relative permittivity

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ABSTRACT

Study is devoted to the effective relative permittivity ε_r of $CeO_2 + x$. Sm_2O_3 thin films prepared by electron-beam physical vapour deposition and ionic beam-assisted deposition methods; ε_r was investigated by three independent ways from the bulk parallel capacitance C_p, impedance capacitance C_{imp}, and accumulation capacitance C_{acc} in dependence on the deposition conditions (deposition temperature, dopant amount x and Ar^+ ion bombardment during the film deposition) used. Investigations were performed using impedance spectroscopy, capacitance–voltage and current–voltage characteristics as well as deep level transient spectroscopy. Results obtained are described and discussed.

1. Introduction

The close relationship between structure/microstructure and electrical as well as mechanical properties of oxide systems with fluorite (F)-type structure influenced by the preparation/deposition conditions is well-known and accepted fact. This fact is usable at looking for new materials/compositions with high ionic conductivity, permittivity and mechanical hardness already at lower temperatures (<700 °C) where these materials can be used as, e.g., electrolytes for the intermediate temperature solid oxide fuel cells (IT-SOFCs) or as catalysts for the acceleration of chemical reactions and also for the other applications at which the high mobility of oxygen ions is important. Besides this, the higher relative dielectric permittivity and high mechanical hardness of these systems are available in microelectronics and for protective coatings. In addition, just doped ceria is interesting material from this point of view. The oxide systems-based on cerium dioxide (CeO_2) belong to the most attractive insulating materials because they are chemically stable, they exhibit a high ionic conductivity under the oxidizing/low-temperature conditions and at higher amounts of dopant, e.g. in the case of trivalent rare earths, such as Sm_2O_3 [1].

The higher relative permittivity ($\varepsilon_r = 26$) [2] and mechanical hardness [3] of these systems, as it was mentioned already above, make them suitable for various applications. These systems can be deposited onto the silicon substrate by e.g. electron-beam physical vapour deposition (EB-PVD) to form a high quality film usable in the silicon-on-insulator structures, stable capacitors for the ultra-large scale integration (ULSI) of electronic circuitry and buffer layers for the epitaxial growth of high-temperature superconductors (HTSC) due to the fact that the mismatch factor for the lattice parameters between CeO_2 and silicon is negligibly low [4]. The higher hardness of these systems is usable at protective coating layers on the metals against corrosion as well as in the planar IT-SOFCs.

The structure and microstructure of Sm_2O_3-doped CeO_2 thin films deposited on silicon substrates by electron beam physical vapour deposition (EB-PVD) and ionic beam assisted deposition (IBAD) methods as well as the frequency and temperature dependences of their *a.c.* conductivity were studied and described in our recent papers [5,6]. The purpose of present study is to complete these investigations by the next chosen electrical and mechanical characteristics from the point of view of applications of these systems as the alternative high-*k* future gate dielectrics and

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protective coatings. The study is focused on the relative permittivity and indentation hardness in dependence on the deposition conditions used and consists of: (1) the study and comparison of effective relative permittivity ε_r obtained using several independent ways, namely from the high frequency limiting capacitance of bulk, C_p and accumulation capacitance, C_{acc} (C–V plots) as well as from the impedance capacitance, C_{imp} (impedance diagrams); the I–V measurements and deep level transient spectroscopy (DLTS) are used for the investigation of dielectric relaxations (the present Part 1) and (2) the indentation hardness, and elastic modulus, H_{pl}/Y, are determined by the indentation technique, namely by the depth sensing indentation (DSI) method, and compared with the results obtained using classical Vickers indentation, HV [6] (Part 2). All investigations are made with respect to the influence of Ar^+ ion bombardment (IBAD) on the mentioned film properties. Part 2 of this study, indentation hardness and elastic modulus, is already accepted for the publication.

2. Experimental

2.1. Sample preparation

The undoped CeO_2 and Sm_2O_3-doped CeO_2 films were deposited by EB-PVD and EB-PVD + IBAD techniques on the stationary Si(1 1 1) and (1 0 0) substrates. The deposition was performed at two temperatures T_{dep} = 200 °C and 500 °C. The deposition rate was ~0.02 nm/s corresponding to $A \sim 10^{15}$ atoms/s/cm^2. A 600 eV Ar^+ ion beam was alternatively used to assist the film deposition. The ion beam current was 2 μA/cm^2 corresponding to $I \sim 10^{15}$ ions s/cm^2. IBAD was used only at T_{dep} = 200 °C. More details about sample preparation can be found in our recent paper [5].

2.2. Electrical measurements

Frequency dependence of the parallel capacitance C_p was investigated at room temperature (RT) and at frequency of 1 MHz using a Solartron SI 1260 impedance/gain phase analyzer with a probing signal of 500 mV amplitude, interfaced to a computer run through a Lab-View program.

Impedance capacitance C_{imp} was investigated similarly as parallel capacitance C_p using a Solartron SI 1260 impedance/gain phase analyzer in the frequency range of 10 Hz–1 MHz and at room temperature up to 120 °C.

Current–voltage (I–V), capacitance–voltage (C–V) in the time domain and isothermal charge deep level transient spectroscopy (DLTS) techniques were used for the measurement of accumulation capacitance C_{acc}. The principle of capacitance measurements in the time domain (measurements in the Feedback-Charge Mode (FCM) [7]) with the sampling events chosen in accordance with the rules published in [8] and the rate window in DLTS are depicted in Fig. 1a–c.

The capacitance is determined by the charge induced as a response to the voltage step ΔU (Fig. 1a). Placing the sampling event at t_1 with respect to the reference level at t_0 determines the total capacitance with the contribution of all relaxation processes with the time constants smaller than t_1: $C = C(0) + C(t_1)$ (Fig. 1b). The sampling time corresponds approximately to the reciprocal value of frequency used at the standard capacitance measurements by a harmonic signal. DLTS technique detects capacitance or charge relaxations due to the charge emission from the defect states or due to the dielectric polarization (Fig. 1c). The basic idea consists of the rate window concept, i.e. transient capacitance or charge is processed by the correlation function $\Delta Q = Q(t_1) - 1.5Q(2t_1) + 0.5Q(4t_1)$ [8]. This function generates a

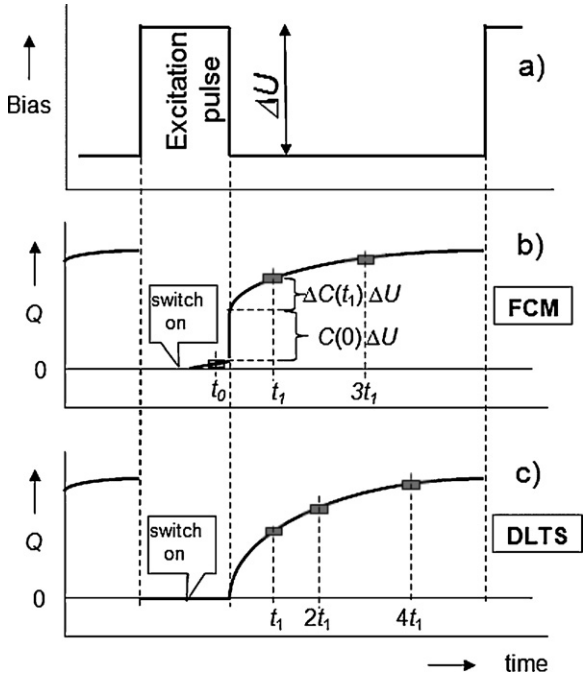

Fig. 1. Timing and sampling sequences relevant to the operation modes of ACTP (Advanced Charge Transient Processor): (a) pulsed bias voltage applied to the sample, (b) capacitance measurement in time-domain performed in the FCM mode (Feedback Charge Mode) and (c) isothermal charge DLTS, where the rate window is swept over the charge transient response.

DLTS peak in the case when a transient signal has a time constant comparable with the sampling time t_1. Therefore the contribution to the total capacitance in time domain can be directly correlated to the relaxation observed with the DLTS. Isothermal DLTS is a modification of original technique where, instead a fixed rate window and sweeping temperature, the relaxation processes are investigated at fixed temperature and rate window is swept.

The capacitance was measured at three different sampling times t_1 (0.1 ms, 1 ms and 10 ms). Isothermal DLTS was measured at the bias voltage, U_b = 0 and $\Delta U = \pm 0.1$ V.

All electrical measurements were performed in air in the metal-insulator-semiconductor (MIS) configuration with aluminum/platinum top contact and gold as the bottom electrode. The top contact was evaporated through the mask and the back contact to Si substrate was deposited by evaporation of Au film. The cell constant of deposited films, $K = t_f/S$, where t_f is the thickness of oxide films and S is the area of gate electrode, was estimated within ±10% of its average value.

3. Results and discussion

3.1. Effective relative permittivity

Electrical conductivity and partially also the relative permittivity ε_r of Sm_2O_3–CeO_2 films deposited on the silicon substrate were investigated recently in our paper [6]. The structure and microstructure of these films in dependence on the preparation conditions used are described in our recent paper [5].

High k-metal oxides in the form of films deposited on silicon substrate such as ZrO_2, HfO_2 doped with aliovalent oxides and also CeO_2-based systems annealed at higher temperatures (>600 °C) in air after their deposition are promising candidates for the gate dielectrics in metal-oxide-semiconductor (MOS) devices [9–13]. The relative permittivity ε_r of Sm_2O_3-doped CeO_2 films