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Massive fabrication of silicon nanopore arrays with tunable shapes

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ABSTRACT

This paper presents an improved wet etching method for the massive production of silicon nanopore arrays. The shape (length-width ratio) of the nanopore can be easily tuned by changing the wet etching mask and controlling the etching time. By adopting silicon on insulator (SOI) wafers, the pore size uniformity of the nanopore arrays was significantly improved. Square and rectangular nanopore arrays with feature pore sizes down to 18 nm were controllably fabricated. Experiments demonstrated that such Si nanopore arrays with tunable pore shapes and sizes can act as reusable stencils for the nanostencil lithography, to directly deposit large-scale ordered arrays of surface micro/nano structures on various substrates with less time and low cost.

1. Introduction

Solid-state nanopores are of great interest for nucleic acid analysis [1–3], lipid bilayers and protein studies [4], molecule separation [5,6], light modulation [7], as well as nanostructure fabrication [8,9]. Since the first fabrication of a solid-state nanpore with true nanometer control using a technique named ion beam sculpting in 2001 [10], a multitude of techniques have been proposed for the fabrication of solid-state nanopores [11]. The most popular techniques nowadays are direct drilling (milling) techniques with either high energy electron beam or focused ion beam (FIB). Direct milling with high energy electron beam is always used to fabricate individual sub–10 nm nanopores in thin membranes including metal oxides [12], SiN_x [13], graphene [14–16], MoS_2 [17] and BN [18]. FIB milling allows for greater flexibility with respect to the dimensions and materials of the membranes, thus, it is predominantly utilized to fabricate nanopores with dimensions of 1–10 nm [19]. However, the direct milling techniques require expensive equipment, such as transmission microscopes (TEMs) or FIBs. In 2015, Khan and Williams proposed a facile and inexpensive method to fabricate an isolated nanopore in a thin silicon membrane, using multistep chemical etching at low concentrations of HF in electrolyte assisted by blue LED illumination [20].

There are also some techniques that can fabricate numerous nanopores simultaneously, such as the track-etching method [21] and the electrochemical anodizing method [22]. Cylindrical and conical pores with dimensions from a few nanometers to several micrometers can be created in polymer membranes using the track-etching method [23]. While the electrochemical anodizing method is widely used to fabricate high-density ($\sim 10^{11}$ pores/cm^2) metal and metal-oxide nanopores [24]. Metal-assisted chemical etching (MaCE) [25] and metal-assisted plasma etching (MaPE) [26] are also used to fabricate massive nanopores in Si membranes. To precisely control the shapes and locations of the nanopores, Han et al. utilized electron beam lithography (EBL) combined with reactive ion etching (RIE) to fabricate neatly ordered nanopores (nanopore array) with uniform pore size of 18 ± 2 nm in silicon dioxide membranes [27,28]. Possible limitations of this technique are the inaccessibility of EBL and RIE, as well as the relatively high cost.

To solve the problem, a three-step wet etching method was proposed to fabricate pyramidal silicon (Si) nanopore arrays in our previous work [29]. Using this method, square Si nanopore arrays with average pore sizes down to 60 nm have been obtained in common Si wafers [30]. In this paper, the generation mechanism of rectangular nanopores with different length-width ratios was carefully analyzed. Silicon on insulator (SOI) wafers were used to improve the pore size uniformity of the nanopore arrays. In addition, nanostencil lithography experiments using the nanopore arrays as reusable templates were performed to directly deposit micro and nano surface pattern arrays.

2. Experiments

P-type (resistivity 1–15 Ω cm), ⟨100⟩ oriented silicon on insulator (SOI) wafers (Shanghai Simgui Technology Co., Ltd. Shanghai, China) were used for the nanopore fabrication. The thicknesses of

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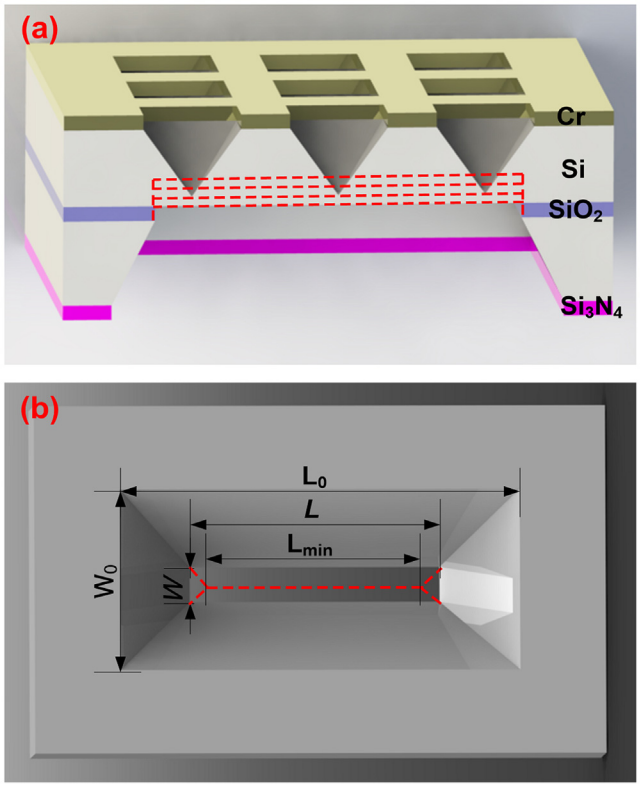

Fig. 1. Schematic illustration of the Si nanopore array fabrication: (a) three-step wet etching of SOI wafer to fabricate pyramidal Si nanopore arrays; (b) the creation of rectangular nanopores with tunable sizes and length-width ratios.

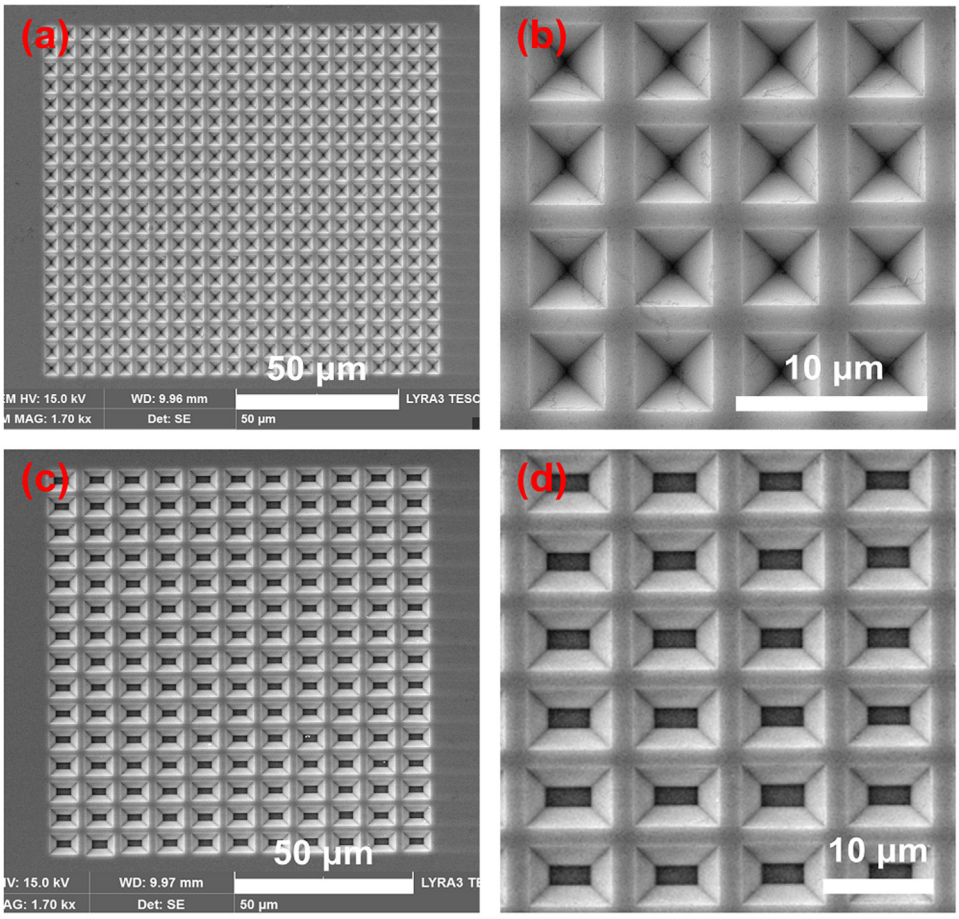

Fig. 2. SEM micrographs of Si pyramidal cavity arrays: (a) and (b) a square pyramidal cavity array and its enlarged details; (c) and (d) a rectangular pyramidal cavity array and its enlarged details.