Applied Surface Science 363 (2016) 296–302

Contents lists available at ScienceDirect

Applied Surface Science

journal homepage: www.elsevier.com/locate/apsusc

Manipulation of stored charge in anodic aluminium oxide/SiO_2 dielectric stacks by the use of pulsed anodisation

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ARTICLE INFO

Article history:
Received 16 May 2015
Received in revised form 3 October 2015
Accepted 9 December 2015
Available online 12 December 2015

Keywords:
Silicon
Stored charge
Surface passivation
Solar cell
Anodic aluminium oxide

ABSTRACT

A method of fabricating anodic aluminium oxide (AAO) with the capability of manipulating its stored charge is reported. This method involves the use of a pulsed current source to anodise aluminium layers instead of the typically used constant current/voltage source, with the test structures experiencing positive and negative cycles periodically. By tuning the positive cycle percentage, it is demonstrated that the effective stored charge density can be manipulated in a range from -5.2×10^{11} to 2.5×10^{12} q/cm^2 when the AAO is formed over a 12 nm SiO_2 layer. An investigation of the stored charge distribution in the dielectric stacks indicates a positive fixed charge at the SiO_2/Si interface, a negative fixed charge at the AAO/SiO_2 interface and a positive bulk charge within the AAO layer. The effective stored charge density and interface states were found to be affected by annealing conditions and it is suggested that oxygen annealing can reduce the bulk positive charge while post-metallisation anneal is most effective in reducing silicon interface defects. Charge manipulation using pulsed anodisation is shown to reduce carrier recombination on boron-diffused silicon surfaces highlighting the potential of the process to be used to tune the electrical properties of dielectric layers so that they can reduce surface recombination on silicon surfaces having different dopant polarity and concentrations.

1. Introduction

The surface passivation for photovoltaic devices is of great importance especially when high efficiency silicon solar cells are being fabricated with thinner substrates [1]. The commonly used passivating dielectrics such as silicon nitride (SiN_x) and aluminium oxide (AlO_x) are capable of providing surface passivation for silicon solar cells due to the combination of both high quality field-effect passivation induced by the dielectric fixed charge, and a low density of interface defects arising from chemical passivation [2–7]. Silicon nitride stores a net positive charge, which enables effective passivation of n^+ surfaces of conventional p-type silicon solar cells. However, the positively charged SiN_x can compromise the passivation on p^+ surfaces as it increases the minority carrier density at the surface [8], and may cause parasitic shunting when applied to p-type surfaces with localised contacts [9]. Consequently, negatively charged AlO_x is preferably used for the passivation of p^+ silicon surfaces.

The selectivity of field-effect passivation on silicon surfaces having different dopant polarity and concentration makes it desirable to be able to controllably manipulate stored charge in dielectric layers. Terlinden et al. [10] have demonstrated tailoring the effective stored charge densities (Q_{eff}) ranging from -6×10^{12} to $+7 \times 10^{11}$ q/cm^2 in AlO_x/SiO_2 dielectric stacks on silicon by varying the SiO_2 interlayer thickness. In another study, Weber et al. [11] reported negatively charged SiN_x formed on p-type silicon surfaces with a Q_{eff} of $\sim -1 \times 10^{12}$ q/cm^2 being achieved using corona discharge. However, no control over the magnitude of the stored charge was demonstrated.

Polarisation of anodic aluminium oxide (AAO) films has been reported [12,13], with this polarisation being attributed to electron-trapping which occurs due to the incorporation of anion impurities in the surface region of the oxide near the electrolyte-oxide interface and a balancing positive charge due to ionic aluminium ion accumulation at the metal-AAO interface. Lambert et al. suggested that the magnitude of this polarisation could be controlled by the use of different anodisation conditions and was correlated with the anion impurity concentration in the surface layers of the oxide [12]. In this paper, we report the use of pulsed anodisation to form AAO

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http://dx.doi.org/10.1016/j.apsusc.2015.12.068
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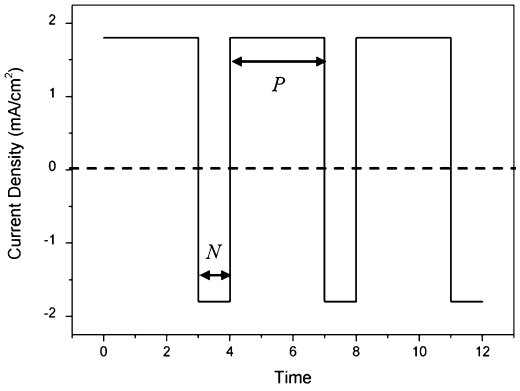

Fig. 1. An example of the current profile for pulsed anodisation with a fixed current density. Note that the P and N denotes the durations of positive and negative cycles respectively.

layers on silicon substrates with the capability to manipulate the magnitude and polarity of the measured Q_{eff}. Anodic aluminium oxide layers were formed on silicon wafers over an intervening SiO_2 layer using a pulsed current source with a periodically changing polarity. It is shown that by tuning the positive cycle percentage (f_p), the magnitude and polarity of Q_{eff} can be controlled. The effect of the thickness of the intervening SiO_2 layer on the effective Q_{eff} is evaluated and a model to explain the distribution of stored charge in the AAO/SiO_2 stacks is proposed. It is shown that different annealing conditions have a significant impact on Q_{eff} and the mid-gap interface defect density (D_{it}) highlighting the complexity of the chemical and electrical processes involved in the pulsed anodisation process. In the final section of the paper, the effect of charge manipulation on the surface passivation of boron-doped silicon surfaces is reported and the results are discussed in relation to the earlier findings in the paper.

2. Experimental

2.1. Sample preparation

Test structures used for stored charge characterisation were p-type Czochralski (Cz) double-side polished 5–10 Ω cm silicon wafers. The wafers were RCA-cleaned, followed by a thermal oxidation at 950 °C to form a SiO_2 layer. Oxidation durations of 10 and 15 min were used to grow SiO_2 layers with a thickness of 12 and 17 nm, respectively (estimated by elllipsometry). The SiO_2 interlayer was used to prevent delamination of the AAO layer from the silicon wafer during anodisation [14]. Aluminium layers with thicknesses varying from 20 to 300 nm were thermally evaporated onto one side of the test structures. Anodisation of the aluminium layers was performed by immersing the test structures in 0.5 M sulphuric acid. During the anodisation, the test structures acted as the working electrode and a nickel plate was used as a counter electrode. A potentiostat from *Ivium Technologies* (model *IviumStat.XRe*) was used to generate a pulsed current with a magnitude of 2 mA/cm^2 and a polarity that changed periodically. Fig. 1 depicts an example of the current profile for a pulsed anodisation with a fixed current density. As shown in Fig. 1, the anodisation current has a periodically changing polarity, with the durations of positive and negative durations denoted as P and N, respectively. The ratio between the positive cycle duration and the cycle length is defined here as the positive cycle percentage (f_p). That is:

$$f_p \equiv \frac{P}{P+N}, \quad (1)$$

For all the experiments reported, the charge manipulation in AAO/SiO_2 stacks was achieved by varying f_p. The other pulsed current parameters, which were kept constant for all experiments, were: (i) a cycle length of 10 s; (ii) current density of 2 mA/cm^2 for both polarities; and (iii) the voltage limit of 30 V for both polarities. The termination of anodisation was indicated by a rapid increase in resistance of the anodisation circuit, manifested as a voltage increase in this case.

The process was terminated when the final voltage stayed unchanged at 30 V for a period of 30 s to ensure complete anodisation. The duration of the anodisation process depended on f_p and the thickness of the aluminium layer. For example, test structures with an aluminium thickness of ~300 nm and anodised with an f_p of 50% required ~580 s to complete the anodisation. For test structures having the same aluminium thickness and anodised using the same f_p, the variation in anodisation time was considered small (<3%).

Annealing can significantly change the Q_{eff} and/or D_{it} of the metal insulator semiconductor (MIS) structures, depending on the types of defects and the annealing conditions [2,15,16]. To better understand the impact of annealing conditions on Q_{eff} and D_{it}, AAO/SiO_2 MIS test structures were annealed in different atmospheres and the impact on Q_{eff} and D_{it} were studied using C–V measurements. Selected test structures anodised at f_p = 80% were annealed in: (i) pure N_2; (ii) 80% N_2 and 20% O_2 mixed atmosphere or; (iii) 5% H_2 and 95% Ar forming gas (FG) at 400 °C for 30 min. A group of test structures were annealed with aluminium pads on the dielectric surfaces, while the other group was annealed before metallisation (i.e., uncapped).

2.2. Characterisation

To characterise the stored charge and interface defects in AAO/SiO_2 stacks, MIS capacitors were fabricated by thermally evaporating a 300 nm aluminium layer through a shadow mask onto the AAO surface to form gate contacts with an area of 0.04 cm^2. On the other side of the test structure, ohmic contacts were fabricated by firstly removing the dielectric on the rear surface (i.e., the surface not of interest to the measurements) of the test structure by fuming in 49 wt% HF, and then depositing an aluminium layer with thickness of ~300 nm onto the bare silicon. Thermal annealing in N_2 ambient at 400 °C for 30 min was used to enhance the quality of ohmic contact. High frequency (1 MHz) capacitance–voltage (C–V) characteristics were measured using an *HP 4194 A* impedance analyzer and the C–V data was corrected for parasitic resistance and inductance. Quasi-static C–V measurements were performed with a linear voltage ramp generated by a HP 4140 B pico-ammeter/dc voltage source. The Q_{eff} in the AAO/SiO_2 stacks was estimated by assuming all the stored charge was located at the SiO_2/Si interface. The metal semiconductor work function difference (ϕ_{ms}) was determined by plotting the flatband voltages as a function of the SiO_2 thickness and finding the intercept at the voltage axis. In the MIS systems described here, the ϕ_{ms} was found to be -0.52 ± 0.03 V. The D_{it} was determined using Castagné's method [17] and/or Terman's method [18].

In order to understand the role of oxygen during annealing in N_2–O_2, X-ray photoelectron spectroscopy (XPS) was performed on the test structures before and after annealing and the measured depth profiles of the O 1s to Al 2p signals were recorded, the ratio of these signals being used as a measure of the oxygen deficiency of the formed layers.

Photoconductance decay (PCD) measurements were used to estimate the recombination current associated with the boron diffused regions (J_{0p+}) from symmetrical test structures to examine the effects of the dielectric stored charge on the surface passivation [19]. The samples used for passivation tests here were planar