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Depth detection and fabrication of porous silicon without the stress

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ABSTRACT

The stress in porous Si could affect the integration of porous Si devices with microelectronic integrated circuits based on silicon. In this paper, aligned macropore arrays without the stress were fabricated by an electrochemical etching procedure under a control voltage. The several etching stages of aligned macropore arrays were examined by microscopic technique, which indicates the variation in morphology from pore nuclei to aligned macropores with branching pores, and finally to aligned macropores without branching pores. Due to the difference of Raman peak positions between porous Si layer and substrate (unetched layer), furthermore, z-scan of Raman spectroscopy which is a nondestructive tool can be used to detect the etching depth. The difference should be ascribed to the quantum confinement of phonons in the porous Si.

1. Introduction

Porous silicon (Si) has attracted increasing interest owing to its wide range of potential application such as photonic, electronic, ultrasonic, biochemical, and energy devices [1–5], since the discovery of its intense luminescence [6]. Porous Si is formed by electrochemical (EC) etching of a crystalline silicon wafer in concentrated hydrofluoric acid solutions under a controlled current. Many experiments present that the skeleton of porous Si keeps the same crystal structure of bulk Si, but with a larger lattice parameter, indicating that the lattice mismatch with the substrate is expected to introduce a compressive stress on the porous film [7–11]. The compressive stress can result in film cracking and peeling [12], which is especially prevalent in radio-frequency applications, because of the very thick insulating layer (>100 μm) required for effective reduction of capacitive and inductive coupling between the various regions of a Si chip [13]. In general, the stress may be studied by high-resolution transmission electronic microscopy (HRTEM) and Raman measurements [4,14].

Raman scattering is a nondestructive tool that is useful in the characterization of semiconductors [15]. The first-order Raman peak (~523 cm^{-1}) in bulk Si is symmetric and has a width of ~3 cm^{-1} (FWHM), whereas porous Si obtained by EC etching under a control current exhibits a wider Raman peak which is very asymmetric, indicating the presence of microcrystalline Si (below ~20 nm) and amorphous Si [16–18]. The above-mentioned issues could affect the integration of porous Si devices with microelectronic integrated circuits based on Si. Furthermore, pore parameters, such as pore depth and pore diameter, also impact the performance of porous Si devices. In general, pore depth which exhibits a nonlinear relationship with the etching time, could be observed by cross-sectional scanning electron morphology (SEM) images [16–21]. However, this technique is a destructive method for the etched samples.

In this paper, we report the fabrication of aligned macropore arrays using an electrochemical etching technique in hydrofluoric acid (HF) under a control voltage. The objective was twofold, i.e., to explore a kind of fabrication method of porous Si without the compressive stress and to provide a new method for nondestructive study on the pore depth of the etched Si wafers.

2. Experimental

Electrochemical porosification experiments were conducted in a two-electrode cell at room temperature with p-type Si cut into 1 cm × 1 cm as the anode and a platinum wire as the counter electrode (cathode) [22]. The resistivity of p-type Si(1 0 0) wafers of 510 μm thickness was 0.5–1 Ω cm. The electrolyte was prepared by adding ethanol to HF (49%) with a volume ratio of 1:1. The anodization process was carried out in a constant voltage of 15 V controlled by a source meter, while etching current was recorded

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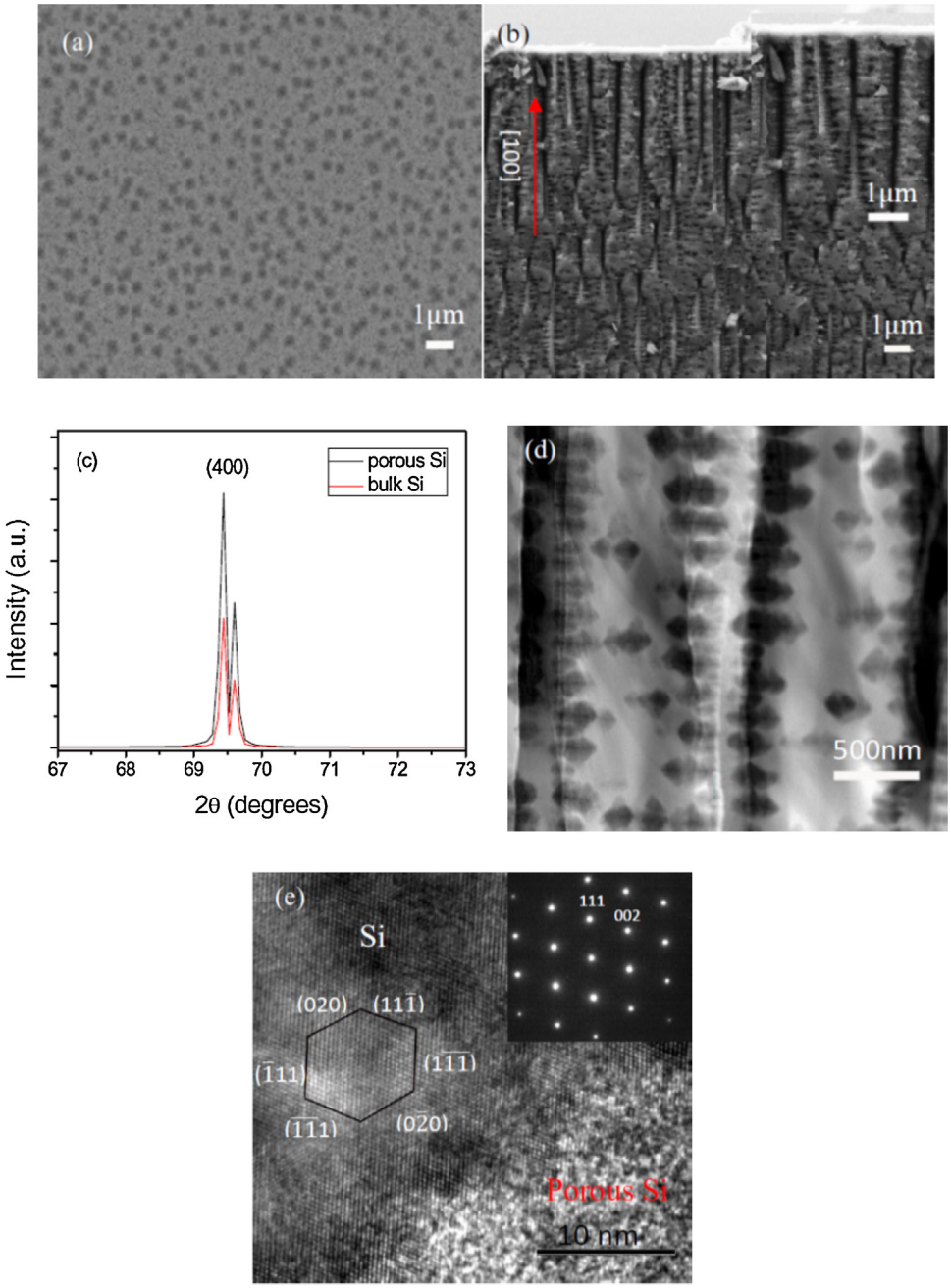

Fig. 1. (a) Top-view and (b) cross-sectional SEM images obtained with a landing electron energy of 5 keV, (c) X-ray (0 0 4) diffraction patterns for (0 0 1) surface, (d) cross-sectional TEM image, and (e) HRTEM image of the etched Si wafers at 15 V for 10 min. The insets in (b) and (e) show the higher magnification image and the corresponding selected area electron diffraction pattern, respectively.

under room light. Scanning electron microscopy (SEM) (Zeiss, SUPRA 55) was used to characterize the morphology of the samples under 5 K electron acceleration voltage. High-resolution transmission electronic microscopy (HRTEM) and X-ray diffraction (XRD) measurements were used to verify the material quality. In the XRD measurements, D8 Advance XRD system with Cu Kα radiation was used. HRTEM and selected area electron diffraction (SAED) were performed on the cross-section sample using a Technai F30 transmission electron microscope operated at 300 kV. Raman spectra of the samples were obtained by the Nexus 670 of Thermo Nicolet with the largest power of 2 W at room temperature using the 785 nm as the exciting source. Photoluminescence (PL) measurements were carried out using the 325 nm solid laser as the exciting source.

3. Results and discussion

Fig. 1(a) and (b) illustrates typical top-view and cross-sectional SEM images of porous Si samples prepared at 15 V for 10 min, respectively. Pore nuclei (pits) with a density of approximately 1.9×10^8 per cm^2 are formed on the surface (Fig. 1(a)). Due to the tendency of the space charge region (SCR) surrounding pore tips to focus mobile charges onto the pore tips, the pore nuclei density can decide pore morphology within the etched layer [19–22]. The width of the SCR can be calculated using Eq. (1)

$$d_{SCR} = \sqrt{\frac{2\varepsilon\varepsilon_0 U}{qN_D}} \quad (1)$$