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Thermal etching of SiC

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ABSTRACT

Thermal etching of SiC or its decomposition at high temperatures is of significance because of the many industrial applications of SiC at high temperatures. The effect of vacuum annealing at relatively high temperatures (1200–1800 °C) on the surface microstructure of 6H-SiC and polycrystalline SiC was investigated using a modern high resolution scanning electron microscope (FEG-SEM) with an in-lens detector. Crystal defects such as stacking faults and twins on the SiC surfaces were easily observed in this system. Thermal etching of SiC already started at 1200 °C with evidence of step bunching and grain boundary grooving. Preferred etching occurred on certain crystal surfaces of polycrystalline SiC. Significant decomposition of SiC occurred at 1800 °C. The resulting decomposition structures have possible nanotechnological applications.

1. Introduction

SiC is a material with many industrial applications even at temperatures above 1000 °C. These applications range from high temperature semiconductor devices, grinding powder, break pads to modern nuclear reactors. Consequently, it is important to investigate the sublimation behaviour and the associated thermal etching as well as the decomposition of SiC at high temperatures in vacuum. Thermal etching is the preferential sublimation of a solid material at sites where the binding energy is lower than at the adjacent areas.

The review paper by Knippenberg [1] summarises the early work on the thermal properties of SiC. It is not possible to melt SiC at atmospheric pressure – it sublimates at high temperatures. At these temperatures its also decomposes into a silicon-rich vapour leaving a graphite layer on the surface in pseudomorphosis of the original crystals. The recent review paper by Snead et al. [2] does not discuss thermal etching directly; it only summarises the thermal decomposition results.

Polycrystalline SiC is usually grown by chemical vapour deposition (CVD) at high temperatures. Like all epitaxial processes, it involves the diffusion of the atoms across the surface of the crystal. Consequently, growth and thermal etching are competing processes occurring simultaneously but with different rates in different temperature regimes [3]. Since the epitaxial growth of SiC is a step-flow mechanism [4] step bunching is a common extended defect of SiC surfaces [5]. According to the Burton, Cabrera, Frank (BCF) [4] and the Frank and van der Merwe theories [6], a crystal grows in layers of thickness equal to the crystal elementary size. The steps move because the adatoms moving under thermodynamical fluctuations usually stick at kink sites. Step bunching is defined as the conglomeration of steps and the formation of multiple-height steps on crystal surfaces. During growth or thermal etching, atoms tend to aggregate and pile up unevenly at steps. Often the steps aggregate together and form step bunches separated by wide terraces. Using TEM, Kimoto et al. [7] found that for 6H-SiC (0 0 0 1) surfaces with an off-axis $\theta = 3.5^\circ$ towards $\langle 1\,1\,2\,0 \rangle$, the step heights are predominantly 3 Si–C bilayer heights. A schematic illustration of step bunching is given in Fig. 1 showing a vicinal crystal surface, i.e. a high Miller index plane making a small angle θ (greatly exaggerated in the figure) with the low index plane (0 0 0 1). Several mechanisms have been proposed for this phenomenon, such as the absorption of impurity atoms on a terrace impeding step advance [8]; or due to the Ehrlich-Schoebel barrier potential at step sites [9]. In general the presence of step bunching formation on crystals is undesirable for applications.

Because the surface energies of the atoms are different at different sites on a crystal [10] the appearance of step bunching on crystal surfaces after high temperature annealing can be taken as evidence of (preferential) thermal etching having occurred during the annealing process.

A review of the papers on thermal etching of SiC shows that the etching depends on the environment. Preferential adsorption/reaction of Si or C with the environment leads to differences in etching rates and morphologies of the surfaces [11–14]. Another observation is that few of the thermal etching studies used SEM. This paper, therefore, endeavors to fill this gap by a high resolution FEG-SEM investigation of polycrystalline and 6H-SiC surfaces after

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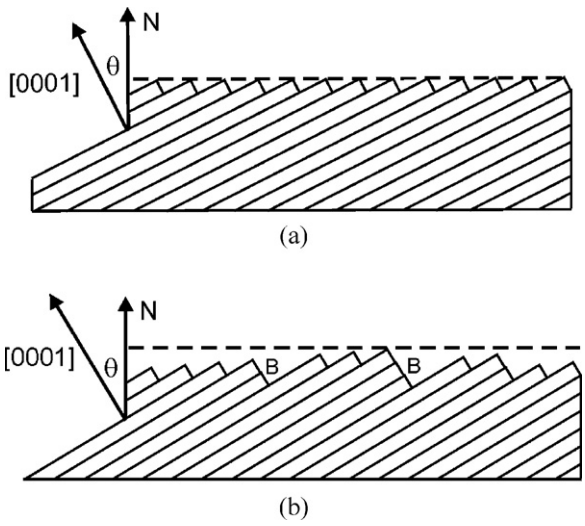

Fig. 1. A schematic illustration of step bunching B on a vicinal single crystal surface. The angle θ is greatly exaggerated. (a) No step bunching. (b) Step bunching.

annealing in vacuum at high temperatures using a modern SEM with an in-lens detector.

2. Experimental

Single crystal 6H-SiC (from *Intrinsic Semiconductors*®) and two sets of polycrystalline SiC – one set from *Valley Design Corporation*® and the other set grown by the CVD process used in the production of the nuclear fuel particles (called TRISO particles) for the South African pebble bed modular reactor (PBMR) reactor (PBMR (Pty) Ltd., Pretoria, South Africa). The substrate for the latter was also a polycrystalline SiC wafer from *Valley Design Corporation*®.

Before annealing, the samples undergone an extended cleaning process. The samples were placed four times in clean boiling acetone for about 4–5 min each time. This was followed by a wash in de-ionised water, and a wash in an Extran (Merck) solution. To remove the soap, the samples were washed three times in de-ionised water. Finally to minimise sticking of a water film on the surface, the samples were rinsed in methanol.

The samples were vacuum annealed in a computer controlled *Webb* graphite furnace for different periods at temperatures ranging from 1200 up to 1800 °C. The base pressure prior to annealing was in the range of 10^{-6}–10^{-7} mbar. During annealing the pressure sharply increased to a maximum of 5×10^{-5} mbar and then decreased to the 10^{-6} mbar range.

The microstructure of the SiC surfaces was investigated by field emission scanning electron microscopy (FEG-SEM) employing a *Zeiss Ultra 55* instrument fitted with the usual SEM detectors and an in-lens detector. This instrument can be operated at voltages as low as 500 eV. In this study we employed 2 kV in order to reduce the distorting effect on very low accelerating voltage SEM images of carbon build-up on the samples during electron beam exposure. With low accelerating voltages the sampling depth becomes smaller giving a more representative picture of the morphology of the real surface. The in-lens detector gives SEM images showing defects present in the samples but at the expense of topographic detail which becomes more detectable with the conventional SEM detector.

3. Results and discussion

It is very difficult to remove mechanical scratch marks due to polishing from SiC surfaces. These scratch marks are usually removed either by H_2 etching [15] or molten KOH etching [16]. As can be seen from the low magnification image in Fig. 2(a), the surface of an as-received polycrystalline SiC sample exhibited numerous scratch marks due to the mechanical polishing by the manufacturer. After annealing at 1200 °C for 60 h in vacuum, much fewer (a reduction of about 2000%) scratch marks were visible due to thermal etching occurring at this relatively low temperature (see Fig. 2(b)). Because of the reduction of scratch marks, the SEM image in Fig. 2(b) is of a lower magnification to show a representative image of the surface. Thus, thermal etching provides an easier alternative than the chemical etching methods quoted above to remove scratch marks and surface damage from polished SiC surfaces. As will be discussed later, the disadvantage of thermal etching as a scratch marks and surface damage removal method is the corresponding increase of surface roughness on polycrystalline SiC.

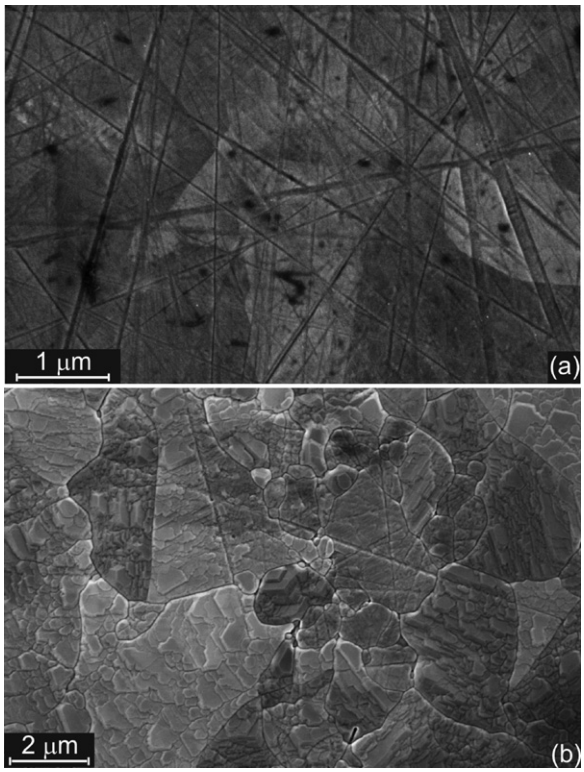

Fig. 2. SEM images of CVD polycrystalline SiC samples. (a) An as-received surface before annealing showing many scratch lines due to a mechanical polishing process. (b) A lower magnification image of the sample annealed at 1200 °C for 60 h in vacuum. Significantly fewer scratch marks are visible.

As was mentioned in the Introduction, a thermal etched surface usually exhibits step bunching. Step bunching was especially visible on single crystalline surfaces as can be seen from Fig. 3. Images (a)–(d) were taken with the in-lens detector which emphases defects such as steps, while (e) is a conventional secondary electron image where topographical features are more visible. The sample was also tilted by 70° with respect to the normal and the SEM was operated at 20 kV. Fig. 3(a) depicts a 6H-SiC sample annealed in vacuum at 1400 °C for 10 h. The effect of an impurity on stopping the movement of steps can be seen in the figure, while the pinning of the step bunches by a micro-hole or micropipe on the same sample is shown in Fig. 3(b). In general, the steps were nearly parallel to each other at this temperature. In contrast, annealing of 6H-SiC at 1500 °C for 30 h caused the steps to be more randomised – see Fig. 3(c). These results can easily be explained by a graph in Ref. [17] showing the ratio of the velocity of kinks moving along a step to the velocity of a step as function of