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Evolution of thin protecting Si-layer on $Mn_{0.5}Si_{0.5}$ layer at low temperatures

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ABSTRACT

Evolution of 2-nm-thick protecting Si-layer on amorphous $Mn_{0.5}Si_{0.5}$ films at elevated temperatures was investigated by using conductive atom force microscopy (CAFM) and other structure and composition characterization methods. At a temperature of 300 °C, a dramatic change was observed in surface morphology with many islands forming on the surface. Those islands were SiO_2 islands rather than Si ones. Further studies showed that those islands formed via first oxidation of the Si cap layer followed by the agglomeration of this SiO_2 layer. Because Si cap layer has widely been used as protecting materials to prevent the surface from oxidizing and contamination, this study provides an insight on the effectiveness of thin protecting Si-layer at low temperatures.

1. Introduction

Surface protection is important for silicon industry, because incorporation of impurities from outside during subsequent processing will change material properties and degrade device performance in a variety of ways, including increasing the leakage current [1,2], changing energy band structures [3] and even having chemical reaction with bulk atoms [4,5]. It is well known that impurities (such as Fe [3], Au [6,7], Pt [6], Ag [7], etc.) will produce deep levels in the band gap of Si and have large capture cross sections for carriers [8], which will greatly degrade the device performances.

For ferromagnetic semiconductor thin films, surface protection is especially important, since oxidation of surface of the films may totally alter their magnetic properties. Thus, a thin protecting cap layer will usually be grown on the top of the materials. For example, thin GaN layer was used to protect dilute magnetic semiconductors (DMSs) p-(Ga, Ni)N [9], a thin BeTe layer for DMSs p-$Be_{(1-x)}Mn_xTe$ [10], a thin ZnSe layer for $Zn_{0.97}Mn_{0.03}Te$ [11], etc.

Si is widely used as a common surface protecting material, since a native thin SiO_2 layer could well prevent further oxidation and is believed to be stable at low temperatures. Also, it is generally thought that a few nanometer-thick Si layer could serve as a good surface protecting layer. In our experiment, a 2-nm-thick Si layer was deposited on amorphous $Mn_{0.5}Si_{0.5}$ as a protecting layer. At the temperature of 300 °C, a dramatic change in surface morphology was observed with many islands forming on the surface. As a result, the protection effectiveness of the Si cap layer degraded. Conductive atom force microscopy (CAFM) results indicate that these islands are SiO_2 islands rather than Si ones. Further studies showed these islands formed via first oxidation of the Si cap layer followed by the agglomeration of this SiO_2 layer, rather than first agglomeration of the Si cap layer followed by oxidation. The possible reasons behind this agglomeration of the SiO_2 layer are discussed.

2. Experiments

P-type Si (0 0 1) substrates with a resistivity of ~20 Ω cm were first cleaned by the Shiraki method and then loaded into an ultra-high vacuum growth chamber (1.0×10^{-9} Torr). The substrates were then heated to 950 °C for 30 min to desorb surface oxide and a clean Si surface with 2×1 reconstruction pattern can be confirmed by reflection high-energy electron diffraction. After that, nearly 8-nm-thick $Mn_{0.5}Si_{0.5}$ film was deposited on Si substrates at room temperature in a molecular beam epitaxy (MBE) system, followed by 2-nm-thick or 8-nm-thick Si cap layer deposition. For comparison, one sample without Si cap layer was also grown at the identical conditions. Samples were annealed in vacuum at different temperatures (namely 200 and 300 °C) for 1 h.

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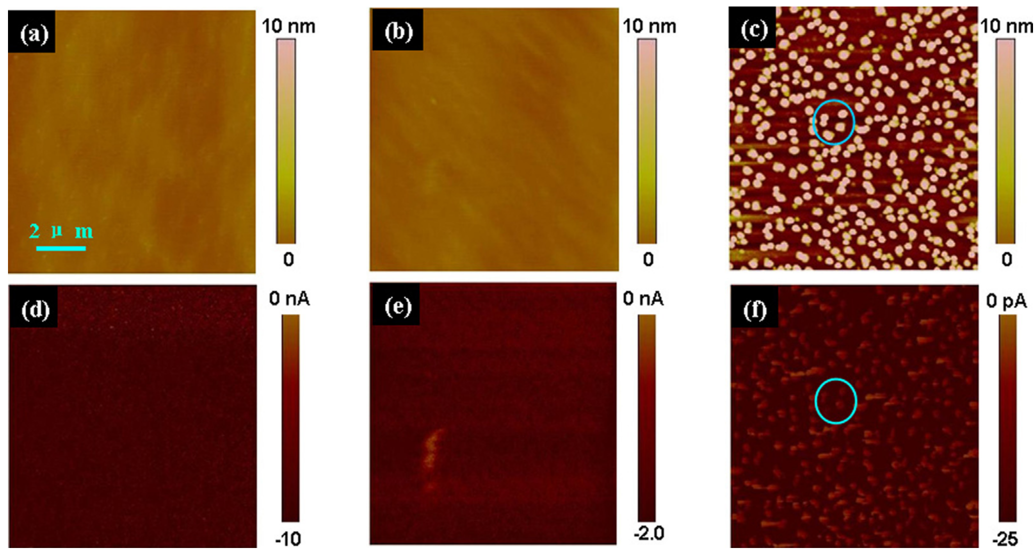

Fig. 1. Topographic and current images of the samples with a 2-nm-thick Si cap layer and annealed at different temperatures taken by CAFM. (a) Topographic and (d) current images of the as-grown sample taken at a sample bias of −3 V. (b) Topographic and (e) current images of the sample annealed at 200 °C taken at a sample bias of −4 V. (c) Topographic and (f) current images of the sample annealed at 300 °C taken at a sample bias of −6 V. All the images are taken at the same size.

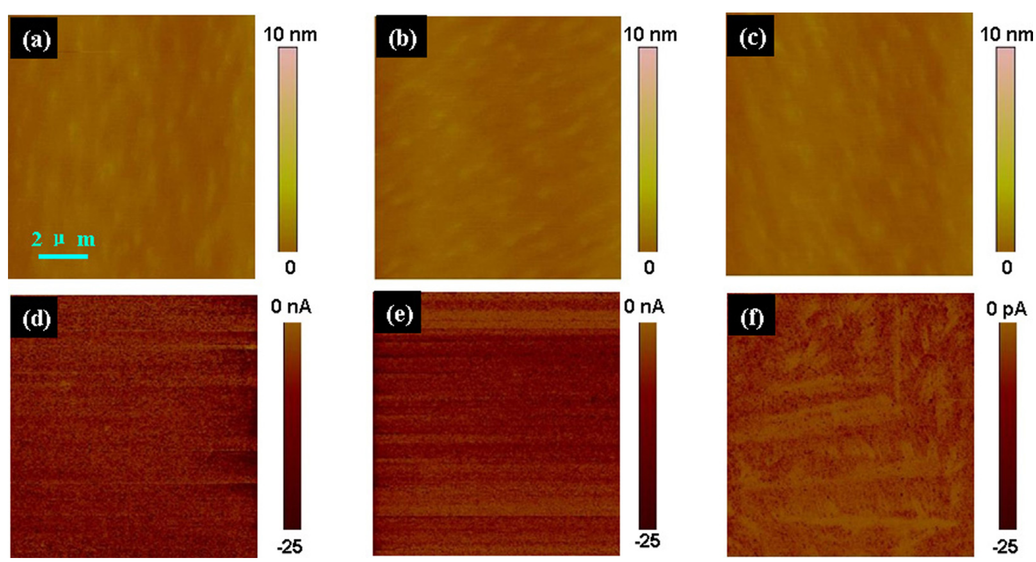

Fig. 2. Topographic and current images of the sample without Si cap layer and annealed at different temperatures. (a) Topographic and (d) current images of the as-grown sample taken at a sample bias of −2 V. (b) Topographic and (e) current images of the sample annealed at 200 °C taken at a sample bias of −2 V. (c) Topographic and (f) current images of the sample annealed at 300 °C taken at a sample bias of −2.5 V. All the images are taken at the same size.

Surface morphologies and electrical conductivities of samples were investigated by a commercial scanning probe microscope (Multimode V, Bruke Nano Surface) in CAFM mode. In this mode, a voltage was applied between CAFM tip and sample, the current image is obtained simultaneously with atomic force microscopy (AFM) image. All the measurements are performed in a nitrogen atmosphere to avoid further oxidation during measurement. Microstructures and composition of samples were characterized by X-ray photoelectron spectroscopy (XPS) (instrument model, AXIS Ultra DLD) and high resolution transmission electron microscopy (HRTEM) (instrument model, FEI Tecani F30).

3. Results and discussion

Fig. 1 shows topography and current images of the samples with 2-nm-thick Si cap layer and annealed at different temperatures. For the as-grown sample, surface roughness is less than 1 nm. The current image is featureless with a current value of −10 nA at an applied voltage of −3 V (Fig. 1d), showing a good uniformity of the sample surface. For the sample annealed at 200 °C, the surface morphology remains smooth (Fig. 1b), however, to obtain the same current, the applied voltage had to be increased to −4 V, which is due probably to a slightly increased thickness of surface SiO_2 layer after annealing (Fig. 1e).

For the sample annealed at 300 °C, a striking change in surface morphology was observed, with appearance of many islands which are 200 nm in diameter and 10 nm in height, as shown in Fig. 1c. The surface of the sample became less conductive, −25 pA at a voltage of −6 V, and the islands became insulating with a much smaller current of −5 pA at the same applied voltage of −6 V, as marked with cycle in Fig. 1f. It implies that those islands may be SiO_2. In order to know what the islands are and how the islands formed, a comparative sample, a $Mn_{0.5}Si_{0.5}$ layer with the same thickness, but without Si cap layer, was grown and annealed under the identical conditions. The surfaces of the as-grown sample and the samples annealed at different temperatures were almost the same, all being