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Elimination of GeO_2 and Ge_3N_4 interfacial transition regions and defects at n-type Ge interfaces: A pathway for formation of n-MOS devices on Ge substrates

G. Lucovsky [a,*], S. Lee [a], J.P. Long [a], H. Seo [a], J. Lüning [b]

[a] North Carolina State University, Department of Physics, Raleigh, NC, USA
[b] Stanford Synchrotron Research Laboartory (SSRL), Menlo Park, CA, USA

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ABSTRACT

The contribution from relatively low-K SiON interfacial transition regions (ITRs) between Si and transition metal (TM) gate dielectrics places a significant limitation on equivalent oxide thickness (EOT) scaling for Si complementary metal-oxide-semiconductor (CMOS) devices. This limitation is equally significant and limiting for Ge CMOS devices. Low-K Ge-based ITRs in Ge devices have also been shown to limit performance and reliability, particular for n-MOS field effect transistors. This article identifies the source of significant electron trapping at interfaces between n-Ge or inverted p-Ge, and Ge oxide, nitride and oxynitride ITRs. This is shown to be an interfacial band alignment issue in which native Ge ITRs have conduction band offset energies smaller than those of TM dielectrics, and trap electrons for negative Ge substrate bias. This article also describes a novel remote plasma processing approach for effectively eliminating any significant native Ge ITRs and using a plasma-processing/annealing process sequence for bonding TM gate dielectrics directly to the Ge substrate surface.

1. Introduction

There has been considerable interest in Ge for applications in scaled complementary MOS (CMOS) devices [1–4], particularly for p-MOSFETs. Many studies have attempted to use Ge native dielectrics, GeO_2, GeON and Ge_3N_4 as interfacial transition regions (IRTs) between the Ge substrate and a high-K dielectric [1–4]. In general, p-metal oxide semiconductor field effect transistors (p-MOSFETs) fabricated on Ge with the Ge-based ITRs and high-K dielectrics; such as HfO_2 and ZrO_2 have yielded acceptable levels of performance for integration into scaled CMOS [3,4], displaying interfacial trap densities in the low to mid 10^{11} cm^{-2} range.

In contrast, (i) our previously reported study of n-MOS capacitors (n-MOSCAPS) with a n-Ge/GeO_2/SiO_2 gate stack structure displayed a density of interfacial charge $>10^{13}$ cm^{-2} [5], and (ii) more recently, n-MOSFETs with Ge_3N_4 or GeON ITRs and high-K HfO_2 and ZrO_2 dielectrics have been *written off* technology roadmaps because of high defect densities, $>5 \times 10^{12}$ cm^{-2}, at the Ge gate dielectric interface [3,4]. None of these studies identified the source of trapping, e.g., a dangling bond. This article identifies the source of this high density of trapped charge as an interfacial conduction band alignment issue in which the conduction band offset for the native Ge dielectric and Ge is smaller than the corresponding conduction band offset for a high-K dielectric such as HfO_2.

This article identifies a novel remote plasma processing approach for effectively eliminating significant native Ge dielectrics ITRs that bridge Ge-high-K dielectric interfaces. Elimination of any significant Ge oxide, nitride or oxynitride ITR has been verified by spectroscopic studies, and is shown to be consistent with markedly improved electrical characterizations. This paper included experimental results that first address (i) gate profiles in Section 2, and then (ii) n-Ge MOSCAPs processing and electrical characterizations in Section 3.

2. Experimental results I: optical band gaps of GeO_2 and Ge_3N_4, and gate stack energy alignment profiles

The O K_1 and N K_1 edges for plasma oxidized Ge and plasma nitrided Ge have been measured, and these were compared, with the respective O K_1 and N K_1 edges of plasma-oxidized and plasma nitrided Ge and Si. Prior to the respective oxidation and nitridation processes, native oxides were removed from the Si and Ge surfaces by conventional wet-chemical etching techniques. Differences between corresponding band edge K_1 edge features in transition metal oxides have been shown to scale linearly with differences in

* Corresponding author.
E-mail address: lucovsky@ncsu.edu (G. Lucovsky).

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optical band gaps determined by spectroscopic ellipsometry, and these correlations carry over to oxide and nitride dielectrics as well [6,7]. Fig. 1(a and b), respectively, are plots that indicate the band edge differences between GeO_2 and SiO_2 in (a), ~3.4 eV, and between Ge_3N_4 and Si_3N_4 in (b), ~0.9 eV. Several studies have determined the optical band gaps of non-crystalline GeO_2 [8–11] and Ge_3N_4 [12]. Based on previously reported values for the band gaps of non-crystalline SiO_2 and Si_3N_4, 8.9 eV and 5.3 eV, respectively, the respective differences obtained from XAS studies, yield band gaps of 5.5 ± 0.1 eV for GeO_2 and 4.4 ± 0.1 eV for Ge_3N_4, in excellent agreement with previous reported values.

The valence band offset energy between Ge and GeO_2 has been determined by ultra-violet photoemission spectroscopy, UPS, and is 3.3 ± 0.15 eV [1]. Combined with a band gap of 5.5 ± 0.1 eV for GeO_2, this yields a conduction band offset energy between Ge and GeO_2 of 1.5 ± 0.15 eV. The valence band offset energy between Ge and Ge_3N_4 has also determined by ultra-violet photoemission spectroscopy, UPS, and is 2.3 ± 0.15 eV [13]. Combined with a band gap of 4.4 ± 0.1 eV for Ge_3N_4, this yields a conduction band offset energy between Ge and Ge_3N_4 of 1.5 ± 0.15 eV.

The measurements of ref. [14] indicate a valence band offset energy between HfO_2 and Ge of about 2.8 ± 0.2 eV. Assuming a band gap of 5.8 ± 0.1 eV for HfO_2, this gives a conduction band offset energy between Ge and HfO_2 of ~2.0 ± 0.2 eV, or about 0.2 eV greater than that between Si and HfO_2 [1,13].

Fig. 2(a) displays the band alignments for n-Ge/GeO_2/HfO_2 and n-Ge/Ge_3N_4/HfO_2 gate stacks using the band gaps and conduction band offset energies note above. This figure demonstrates that when GeO_2 and Ge_3N_4 are used as ITRs between Ge and HfO_2, the band gaps of these ITRs are *less than* that of the high-K HfO_2 dielectric. These gate stack alignments are qualitatively different than those for Si gate stacks with SiON ITRs where the band gaps of the ITRs are *greater than* that of HfO_2. Fig. 2(b) compares injection from an n-type Ge substrate for a Ge/GeO_2/HfO_2/Al metal gate stack, in which the conduction band offset energy between Ge and GeO_2 is *less than* the conduction band offset energy between Ge and HfO_2 in with that for a n-Si/SiON/HfO_2/Al metal gate stack, in which the conduction band offset energy between Si and SiON ITR is greater than the conduction band offset energy between Si and SiO_2. Under these bias conditions, and independent of the gate metal, Al or mid-gap TiN, there is a *potential well* or *electron trap* in the GeO_2 film between the n-type Ge substrate and HfO_2 that is active when a negative bias is a applied to n-type Ge, or when a p-type Ge substrate is inverted by the application of a large negative bias, as in an n-MOSFET. Substrate current injection is qualitatively different for band alignment for an n-Si/SiON/HfO_2/Al metal gate stack for which the ITR band gap is *greater than* that of HfO_2. Qualitatively similar band alignment diagrams apply when either SiO_2, or a high Si_3N_4 content Hf Si oxynitride dielectric replaces HfO_2.

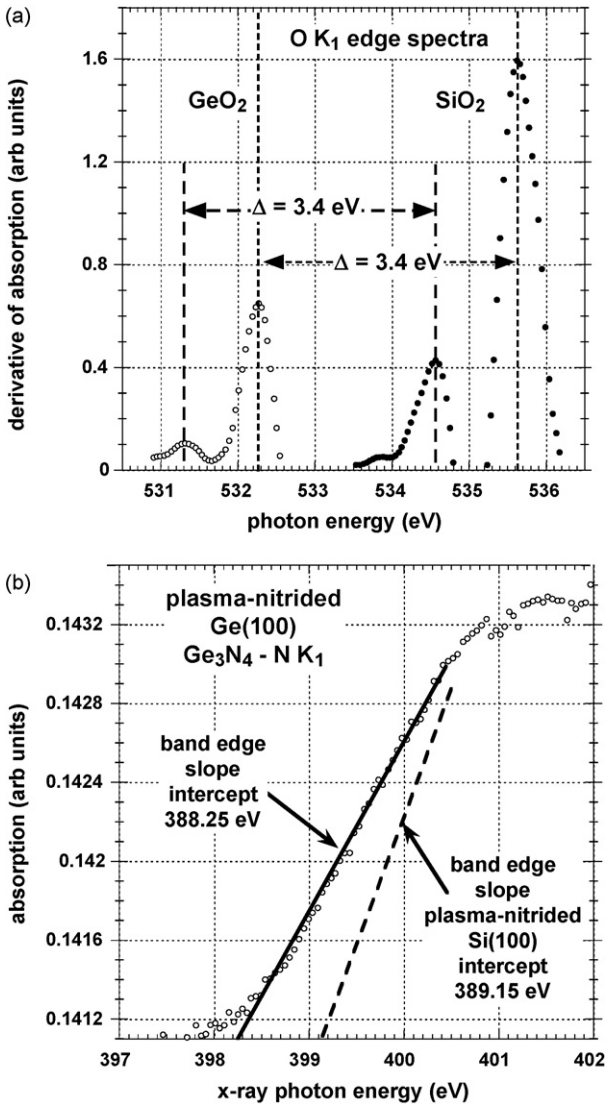

Fig. 1. (a) Comparison between O K_1 derivative absorption spectra for plasma-oxidized Ge and Si, i.e., for GeO_2 and SiO_2 and (b) comparison between N K_1 absorption spectra for plasma-nitrided Ge and Si, i.e., for Ge_3N_4 and Si_3N_4.

3. Experimental results II: gate stack formation and electrical measurements

Thin films on HfO_2 and a high Si_3N_4 content Hf Si oxyntride pseudo-ternary alloy, $(HfO_2)_{0.3}(SiO_2)_{0.3}(Si_3N4)_{0.4}$, have been

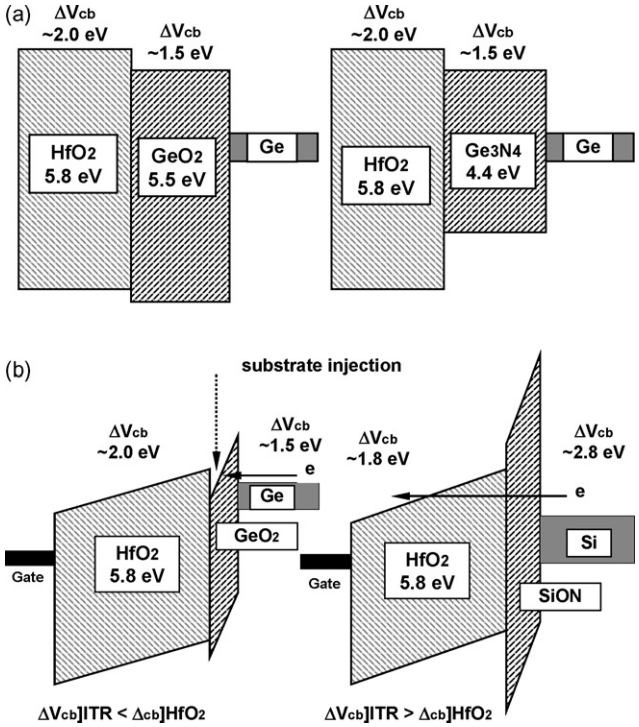

Fig. 2. (a) Band alignments between (i) n-type Ge, GeO_2 and HfO_2 and (ii) n-type Ge, Ge_3N_4 and HfO_2 and (b) substrate injection for an n-type Ge, GeO_2 and HfO_2 stack in (a), with and Al gate electrode, for which the conduction band offset energy between Ge and GeO_2 which is *less than* that between Ge and HfO_2, and for a gate stack on n-Si and with an SiON ITR, which is *greater than* that between Si and HfO_2.