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A study of interface characteristics in HfAlO/p-Si by deep level transient spectroscopy

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ABSTRACT

Deep level transient spectroscopy (DLTS) and high-frequency capacitance–voltage (HF-CV) measurement are used for the investigation of HfAlO/p-Si interface. The so-called "slow" interface states detected by HF-CV are obtained to be 2.68×10^{11} cm^{-2}. Combined conventional DLTS with insufficient-filling DLTS (IF-DLTS), the true energy level position of interfacial traps is found to be 0.33 eV above the valance band maximum of silicon, and the density of such "fast" interfacial traps is 1.91×10^{12} cm^{-2} eV^{-1}. The variation of energy level position of such traps with different annealing temperatures indicates the origin of these traps may be the oxide-related traps very close to the HfAlO/Si interface. The interfacial traps' passivation and depassivation effect of postannealing in forming gas are shown by comparing samples annealed at different temperatures.

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1. Introduction

To reduce gate leakage current, high-k materials have been under investigation as potential replacements of SiO_2 for gate dielectrics in future complementary metal-oxide-semiconductor (CMOS) technology [1]. Among various oxides considered, HfO_2 is regarded as a very promising one. To limit its disadvantages such as low crystallization temperature and poor thermal stability, many groups have been focused on incorporating HfO_2 with aluminum [2–4]. Compared with HfO_2 films, HfAlO alloy retains amorphous up to 1000 °C [2], which is much higher than HfO_2's crystallization temperature. In addition, the thermal stability also improves significantly.

Unfortunately, few works have been done on the properties of the interfacial traps at HfAlO/Si interface in details. The knowledge of electronic structure of the interface is a key to the understanding of the electrical reliability and mobility degradation, and measurement of these interfacial states also provides essential information for predicting device performance. This is more important when the interfacial region becomes the dominant part of MIS structure with the decrease of the insulator thickness. In this paper, the characterizations of the HfAlO/Si interface are investigated by HF-CV and deep level transient spectroscopy (DLTS). By combined conventional DLTS with insufficient-filling DLTS (IF-DLTS), the energy level position of interfacial traps and the activation energy of capture cross-section are obtained as $E_v + 0.33$ eV and 0.11 eV, respectively. In addition, to know the effects of postannealing on the electrical properties of HfAlO films, samples are annealed under different conditions. The change of interfacial traps density (D_{it}) and activation energy of interfacial traps are investigated by comparing the DLTS signals of different samples.

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2. Experiment

The p-type Si(1 0 0) (doping concentration of 8.9×10^{15} cm^{-3}) was cleaned by standard RCA method followed by 1 min dipping in dilute HF solution to remove native oxide layer. Then HfAlO film was deposited in atomic layer deposition (ALD) system by using $Al(CH_3)_3$ (TMA), $Hf(NCH_3C_2H_5)_4$ (TEMAH) and H_2O as precursors. The deposition procedure was 1.5 s TMA pulse followed by 2.5 s N_2 purge, 1.0 s H_2O pulse followed by 3.0 s N_2 purge, and then 5.0 s TEMAH pulse followed by 10 s N_2 purge, 1.0 s H_2O pulse followed by 3.0 s N_2 purge. It was repeated for 12 cycles. After the growth of HfAlO films, aluminum was deposited and the active area is 7.744×10^{-3} cm^2. Samples were annealed at different temperatures (300 °C, 375 °C, and 450 °C, respectively) for 15 min in forming gas (FGA:H_2:N_2 = 5:95).

Capacitance–voltage (C–V) measurements were carried out at room temperature by HP 4284 LCR meter controlled by computer. Measurement of DLTS was performed by Boonton 7200 capacitance meter, and transient capacitance signals were displayed and digitally stored by HP 54600B oscilloscope in the temperate range between 77 K and 340 K.

3. Results and discussion

Fig. 1 depicts the C–V characteristics of the as-deposited sample when the test frequency is 1 MHz, and the scanning speed is 0.03 V s^{-1}. Through the capacitance in accumulation region, equivalent oxide thickness (EOT) is calculated to be about 4 nm. The relative permittivity is estimated to be 11.7 by the comparison of physical thickness of films measured by transmission electron microscopy (TEM). The hysteresis behaviors of C–V curves are performed by changing the direction of voltage scanning which is indicated by the arrows in Fig. 1. The main cause of such hysteresis is the existence of the so-called "slow" interface states, and the density of these states can be determined by the equation as follows [5]:

$$N_{it} = \frac{C^*_{ox} V_h}{q}, \tag{1}$$

where C^*_{ox} is the oxide capacitance per unit area, V_h is hysteresis shift of voltage (it is 50 mV in Fig. 1), and q is the electron charge. The calculated density of "slow" interface state is about 2.68×10^{11} cm^{-2}.

To detect the "fast" interfacial traps, samples are initially biased into accumulation region in DLTS measurement, and those traps with energy E_T above Fermi level will be filled with majority holes. After pulse, the bias switches to inversion region, those traps will emit holes to valence band with emission rate e_p, which is given by [6]:

$$e_p = \sigma_p \nu_{th} N_V \exp\left[-\frac{E_T - E_V}{kT}\right] = \gamma_p \sigma_p T^2 \exp\left[-\frac{E_T - E_V}{kT}\right], \tag{2}$$

where σ_p is the hole capture cross-section, ν_{th} is the thermal velocity of holes, N_v is effective density of state of hole in valence band, and γ_p is the constant.

Capture cross-section σ_p follows this relationship [6,7]:

$$\sigma_p = \sigma_\infty \exp\left(-\frac{E_b}{kT}\right), \tag{3}$$

where σ_∞ is the capture cross-section at $T -> \infty$, E_b is active energy of capture cross-section.

Substituting Eq. (3) into Eq. (2) gives

$$e_p = \frac{1}{\tau} = \gamma_p \sigma_\infty T^2 \exp\left[-\frac{\Delta E_h}{kT}\right], \tag{4}$$

where $\Delta E_h = (E_T - E_V) + E_b$, ΔE_h is active energy of traps. e_p can be obtained by selection of the "rate window" t_1 and t_2 in DLTS measurement, and is given by

$$e_p = \frac{\ln(t_2/t_1)}{t_2 - t_1}, \tag{5}$$

Through changing t_1 and t_2, we can obtain Arrhenius plot of $\ln(e_p/T^2)$ versus $1/T$. Active energy ΔE_h and capture cross-section σ_∞ are determined by the slope and intercept of Arrhenius plot, respectively.

Fig. 2 shows the DLTS spectra of the as-deposited sample with quiescent voltage V_q of 1 V, pulse voltage V_p of −2 V and pulse width of 10 ms. Corresponding Arrhenius plot is shown in the inset of Fig. 2 when the t_1(ms)/t_2(ms) = 20/80, 40/160, 60/240, 80/320, and 100/400, respectively. It can be seen that the DLTS signal is caused by majority carriers, active energy ΔE_h and capture cross-section σ_∞ are found to be 0.44 eV and 4.333×10^{-19} cm^2, respectively. The interfacial traps density D_{it} can be calculated by [7]:

$$D_{it} = -\frac{\varepsilon_{si} N_A}{kT \ln(t_2/t_1)} \frac{C^*_{ox}}{C^3_{hf}} \Delta C_{max}, \tag{6}$$

where ε_{si} is the permittivity of Si, N_A is the doping concentration of Si substrate, C_{hf} is the capacitance per unit area when $V = V_q$, ΔC_{max}

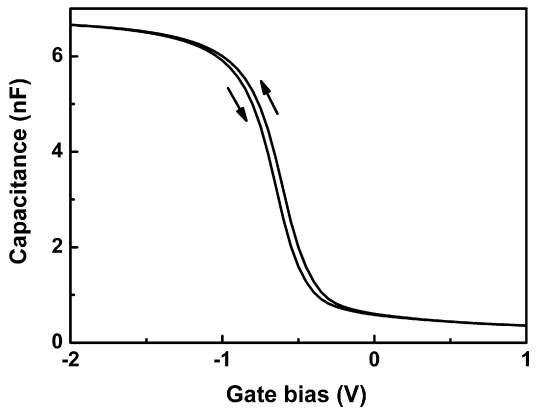

Fig. 1. C–V curves of the as-deposited sample at 1 M Hz.

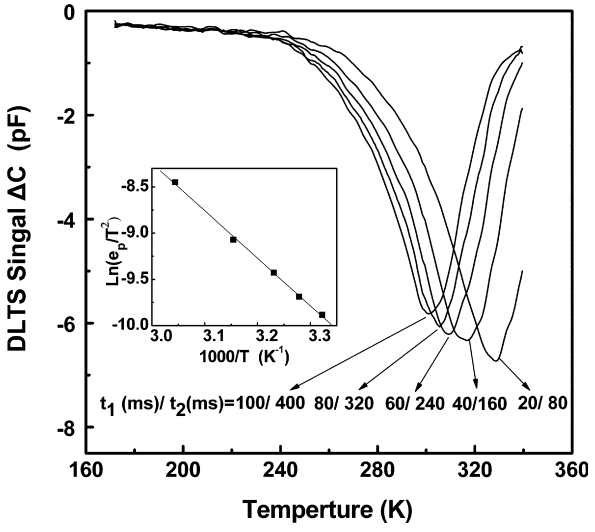

Fig. 2. The conventional DLTS spectra of the as-deposited sample when different rate windows are chosen.

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