



Annealing effect on Schottky barrier inhomogeneity of graphene/n-type Si Schottky diodes

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ARTICLE INFO

Article history:

Received 21 February 2014

Received in revised form 3 April 2014

Accepted 9 May 2014

Available online 17 May 2014

Keywords:

Graphene

Si

Interfacial property

Electrical property

Schottky barrier height

ABSTRACT

The current–voltage characteristics of graphene/n-type Si (n-Si) Schottky diodes with and without annealing were measured in the temperature range of -120 to 30°C and analyzed on the basis of thermionic emission theory. It is found that the barrier height decreases and the ideality factor increases with the decrease measurement temperatures. Such behavior is attributed to Schottky barrier inhomogeneities. It is shown that both the barrier height and the ideality factor can be tuned by changing the annealing temperature. Through the analysis, it can be suspected that a SiO_x layer at the graphene/n-Si interfaces influences the electronic conduction through the device and stoichiometry of SiO_x is affected by annealing treatment. In addition, both Schottky barrier inhomogeneity and the T_0 effect are affected by annealing treatment, implying that stoichiometry of SiO_x has a noticeable effect on the inhomogeneous barriers of graphene/n-Si Schottky diodes.

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1. Introduction

Graphene is a zero-gap semiconductor and has a very large intrinsic carrier mobility, which makes it a very promising material for incorporation into devices ranging from diodes to transistors [1–9]. Due to the technological importance of Schottky diodes which are among the most simple of the graphene-Si contact devices, a full understanding of the nature of their electrical characteristics is of great interest. In this paper, we report the electrical properties of graphene Schottky contact on the n-type Si (n-Si) film. In recent years, solar cells, diodes and memory devices based on Si have attracted great interest [8,10–19]. Si has been a popular material of choice because it is very abundant, non-toxic, and has a rich history in advanced electronics. However, due to the heterojunction nature, the interface is very important and can easily form defects that can diminish the device performance. Given the proper application of an interlayer between the graphene and n-Si interface, the defect density located inside the depletion region of graphene/n-Si diode can be reduced. On the other hand, it was suggested that charge puddles may be responsible for the presence of inhomogeneous barrier heights in the graphene/Si Schottky diodes, which property still remains not fully understood [9]. A simple technique (that is, annealing with different temperatures) to

find the inhomogeneous barriers of graphene/n-Si Schottky diodes was developed in this study. Correlation effects were evaluated using the well-known expression for the thermionic emission (TE) [8,12,15,17]. Based on the expression, the ideality factor (η) and Schottky barrier height ($q\phi_B$) of graphene/n-Si Schottky diodes were extracted in this study. η and $q\phi_B$ are critical parameters that influence device efficiency by controlling charge transport across interfaces. By analyzing these experimental results, we shall discuss on the possible sources of Schottky barrier inhomogeneity.

2. Experimental procedures

Four-inch n-Si (100) wafers with resistivity in the range of $1\text{--}10\ \Omega\text{ cm}$ purchased from Woodruff Tech Company were used in the experiment. The n-Si film thickness was about $525\ \mu\text{m}$. The n-Si samples were cleaned in chemical cleaning solutions of acetone and methanol, rinsed with de-ionized water, and blow-dried with N_2 . Next, the n-Si sample was chemically etched with a diluted HF solution for 1 min, rinsed with de-ionized water and blow-dried with N_2 . The graphene thin films were prepared by chemical vapor deposition (CVD) method. Before the CVD growth of graphene, the copper foil ($90\ \mu\text{m}$ thick) was preannealed at 1000°C for 30 min under a flow of $\text{H}_2 = 9\text{ SCCM}$ (SCCM denoted standard cubic centimeter per minute) in order to prepare a high-density terrace structure on Cu. A gas mixture of CH_4 (120 SCCM) and H_2 (40 SCCM) was used for the growth of graphene at 66.7 Pa [20]. After 40 min of growth, the system was cooled to room temperature under H_2 . To

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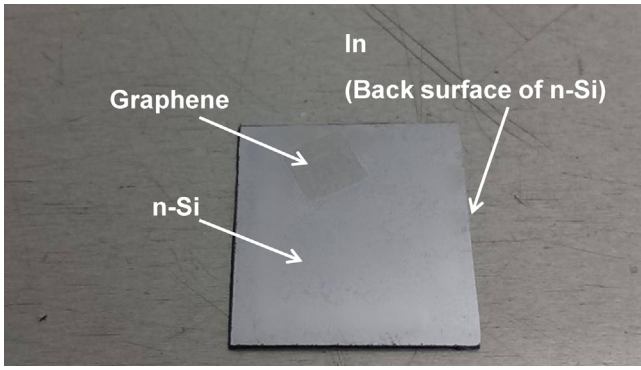


Fig. 1. An optical picture of the graphene/n-Si sample.

transfer the as-grown graphene sheets, a polymethylmethacrylate (PMMA) layer was spin coated on the graphene/Cu sample. The PMMA/graphene/Cu sample was then baked at 100 °C for 1 min. The procedures from coating to drying were repeated 5 times. Next, the sample was immersed in FeCl₃ solution (0.1 g/cm³) for 6 h overnight to remove the Cu substrates. The PMMA/graphene layers were respectively transferred to n-Si substrates, and the PMMA layer was finally dissolved by acetone. The graphene/n-Si samples were then dried at 50 °C for 30 min in air. In ohmic contacts were deposited onto the back surface of n-Si by a sputter coater. Fig. 1 shows an optical picture of the graphene/n-Si device. Some of graphene/n-Si devices were then inserted into a furnace and annealed in pure nitrogen ambient for 1 min. The annealing temperature was varied from 200 to 400 °C, with an error of 0.2%, taking advantage of the temperature profile of the furnace. The current–voltage (*I*–*V*) curves were measured using a Keithley Model-4200-SCS semiconductor characterization system. The *I*–*V* characteristics of the devices were measured in the temperature range of 100–500 K using a temperature controlled cryostat. Techniques to transfer graphene onto various substrates are known to induce disorder, vacancies and impurities at the graphene surface. The structural property of graphene was examined using Raman spectroscopy (Ramboss 500i, DongWoo Optron). A 532-nm laser was used for excitation. Raman spectroscopy is a powerful tool to investigate the structural aspects of carbon-based materials. To understand the improved device performance by annealing, the C 1s and Si 2p core levels of the non-annealed and annealed graphene/n-Si samples were analyzed using X-ray photoelectron spectroscopy (XPS). XPS measurements were performed using a monochromatic Al K α X-ray source. The photon energy was calibrated with the Au 4f core-level line. Curve fitting of the C 1s and Si 2p spectra was performed using a Gaussian–Lorentzian peak shape after performing a Shirley background correction.

3. Results and discussion

Fig. 2 shows the Raman spectra of the graphene/Cu and graphene/n-Si samples, respectively. As shown in Fig. 2, graphene displays a band at $\sim 1345\text{ cm}^{-1}$, a band at $\sim 1580\text{ cm}^{-1}$ and a band at $\sim 2700\text{ cm}^{-1}$ corresponding to the well-documented D, G and 2D bands [4,7,21]. The G band is assigned to the E_{2g} mode of the relative motion of sp² carbon atoms. The amount of disorder in graphene is often correlated with the intensity of the D band [4]. The shape of the 2D band is related to the layer numbers of graphene. The peak intensity for the 2D peak is similar to that for the G peak, suggesting that four layers of graphene formed [22,23]. There were no observable changes in the Raman spectra of graphene/Cu and graphene/n-Si samples, implying that techniques to transfer graphene onto Si substrates did not induce disorder in graphene.

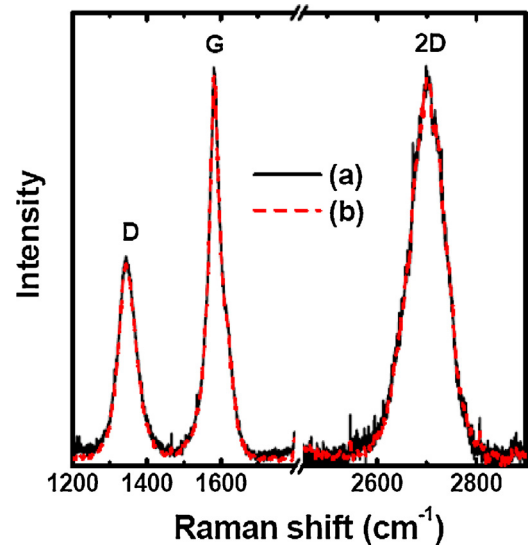


Fig. 2. Raman spectra of (a) graphene/Cu and (b) graphene/n-Si samples.

Fig. 3(a) shows the *I*–*V* characteristics of non-annealed, 200 °C-annealed and 400 °C-annealed graphene/n-Si devices at 30 °C, respectively. The rectifying *I*–*V* characteristics suggest that Schottky junctions are formed at the non-annealed and annealed graphene/n-Si interfaces. Fig. 3(b)–(d) shows the temperature-dependent forward-bias *I*–*V* characteristics of non-annealed, 200 °C-annealed and 400 °C-annealed graphene/n-Si devices in the temperature range from –120 to 30 °C by steps of 30 °C. From TE theory, the forward-bias *I*–*V* characteristic of a Schottky diode is given by [8,12,15,17]

$$I = I_s \left[\exp \left(\frac{qV}{\eta kT} \right) - 1 \right] = SA^* T^2 \exp \left(-\frac{q\phi_B}{kT} \right) \left[\exp \left(\frac{qV}{\eta kT} \right) - 1 \right] \quad (1)$$

where S ($S = 0.04\text{ cm}^2$) is the graphene area, q is the electron charge, T is the measurement temperature, k is the Boltzmann constant and A^* is the effective Richardson constant ($114\text{ A cm}^{-2}\text{ K}^{-2}$ for n-Si) [17]. η is determined from the slope of the linear region of the forward-bias $\ln(I)$ –*V* characteristics through the relation;

$$\eta = \frac{q}{kT} \left[\frac{dV}{d(\ln I)} \right] \quad (2)$$

From the curve fitting of *I*–*V* characteristic, η and $q\phi_B$ were extracted. Fig. 4 shows η ($q\phi_B$) as a function of temperature. In agreement with the previously reported results for graphene/n-Si Schottky diodes [3,6,7,24], we found that the extracted room-temperature $q\phi_B$ values were varied in the range of 0.67 to 0.74 eV. For non-annealed and annealed graphene/n-Si devices, $\eta > 2$ is found at different measurement temperatures, suggesting that interface states may play important roles in the conduction process. However, annealing may lead to reduced η and increased $q\phi_B$, implying that the sensitivity of interface states to annealing provides an opportunity to tune electrical parameters of graphene/n-Si Schottky diodes. In addition, in Fig. 4, we can see that $q\phi_B$ decreases and η increases with the decrease measurement temperatures. Such behavior is attributed to Schottky barrier inhomogeneities. This implies that interface states have noticeable effect on Schottky barrier inhomogeneity for graphene/n-Si diodes. According to the Tung's model [25], both the ideality factor of more than 1 and its linearity versus $10^3/T$ can be convincing evidence of an inhomogeneous barrier. In addition, the variation in η with temperature is called the T_0 effect [26]. Fig. 5 shows η as a function of $10^3/T$, showing that the $\eta - (10^3/T)$ curve is very linear. Such behaviors of

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