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Investigating the effects of the interface defects on the gate leakage current in MOSFETs

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ABSTRACT

The effects of the interface defects on the gate leakage current have been numerically modeled. The results demonstrate that the shallow and deep traps have different effects on the dependence relation of the stress-induced leakage current on the oxide electric field in the regime of direct tunneling, whereas both traps keep the same dependence relation in the regime of Fowler–Nordheim tunneling. The results also shows that the stress-induced leakage current will be the largest at a moderate oxide voltage for the electron interface traps but it increases with the decreasing oxide voltage for the hole interface traps. The results illustrate that the stress-induced leakage current strongly depends on the location of the electron interface traps but it weakly depends on the location of the hole interface traps. The increase in the gate leakage current caused by the electron interface traps can predict the increase, then decrease in the stress-induced leakage current, with decreasing oxide thickness, which is observed experimentally. And the electron interface trap level will have a large effect on the peak height and position.

1. Introduction

Structure defects in crystalline and amorphous silica play an important role in the performance of microelectronics devices. Understanding the microscopic origin effects in MOSFETs (metal–oxide–semiconductor field effect transistor) can guide modifications of the fabrication process and yield devices that can reliably be extended to smaller structure. The point defects in silica will result in the localized states introduced into the band gap of silica. They are potentially the sources of the gate leakage current. As lateral transistor dimensions are scaled into the nano-scale to achieve high levels of speed and integration, there must be corresponding decreases in the gate oxide-equivalent thickness to maintain current levels required for circuit operation. Leakage current through an ultra-thin gate oxide due to defect-mediated tunneling and quantum-mechanical direct tunneling is increasingly becoming an important aspect of device operation in the nano-scale MOSFET technology. Leakage current through the gate dielectric due to direct tunneling becomes a severe problem even at low operating voltages when the physical dimensions of transistors are scaled down to nano-scale.

A major concern in silicon technology is the reliability of CMOS (complementary metal–oxide–semiconductor) devices while they are scaled to smaller dimensions. Stress-induced leakage current can be regarded as a major dielectric reliability concern and has been extensively studied, e.g. [1–9]. But the conduction mechanism for the stress-induced leakage current still remains an area of much discussion. For example, Scarpa et al. showed that oxide positive charge trapping during constant current stress and stress-induced leakage current have the same generation kinetic [1]; Goguenheim et al. observed that hot electrons have little effects on stress-induced leakage current generation in metal–oxide–semiconductor field effect transistor during channel hot carrier injection stresses [2], a capture cross-section as large as 10^{-13} to 10^{-14} cm^2 for the generated acceptor like trap and a smaller capture-cross section in the region of 10^{-15} to 10^{-16} cm^2 have been reported in Ref. [3]. The hypothesis that the neutral trap-assisted tunneling is a source of the stress-induced leakage current gains a wider acceptance. Therefore, it is necessary to investigate that the correlation between the interface defects and stress-induced leakage current.

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2. Methods

For the defect oxide, the tunneling has been regarded as an electron transition from the electrode (gate or substrate) to the traps in the gate oxide, then from the traps to the electrode (substrate or gate). As we know that there are two important parameters for a trap. One is the trap level and the other is the capture cross-section. The capture cross-section means the cross section for electron or hole captured by a trap in a gate oxide. And the location of the trap within the band gap of the gate oxide can be obtained according to trap level. Therefore, the trap states has been treated as some local states within the band gap of silica existed at the interface, and such local states will have capture lengths along the tunneling direction around the defect center. The capture length can be determined according to the square root of the capture cross-section of trap. Therefore, two-step tunneling occurs: the first, from the substrate (gate) to the traps, the second, from the traps to the gate (substrate). It is somewhat like a potential well with the depth being the trap level and the width being the capture length that is introduced in the conduction band of gate oxide. In order to calculate the tunneling current through the gate oxide with traps, firstly, the gate oxide has been divided into to many small parts in the x–y plane that is perpendicular to the tunneling direction. The traps in the gate oxide have been assumed not to be interacted each other in this work. For the gate oxide with one trap, it can be divided into two parts: one with the volume that the area in the x–y plane equals the capture cross-section is defect oxide, the left is the perfect oxide. Thus, these regions are basically composed with two types: one is the perfect oxide; the other is defect oxide. Then the tunneling current through the total gate oxide can be calculated.

The tunneling currents can be calculated using the following expression [10]:

$$J = \int_0^\infty \frac{qm_z^*}{2\pi^2\hbar^3} D(E_z) \left(\int_{E_z}^\infty [f_r(E) - f_l(E)]\, \mathrm{d}E \right) \mathrm{d}E_z \tag{1}$$

The transmission coefficient $D(E_x)$ can be calculated by a numerical solution of the one-dimensional Schrödinger equation. A parabolic $E(k)$ relation with an effective mass m^* has been assumed in this work. The barrier has been discretized by N partial subbarriers of rectangular shape that cover the whole gate oxide layer. From the continuity of wave-function and quantum current density at each boundary, the transmission coefficient through the gate oxide is then found by

$$D(E_x) = \frac{m_0}{m_{N+1}} \frac{k_{N+1}}{k_0} \frac{|\det M|}{|M_{22}|^2} \tag{2}$$

where M is a (2×2) product matrix, M_{22} is the quantity of the second row and the second column in this matrix $M = \prod_{l=0}^{N} M_l$ with transfer matrices M_l given by

$$M_l = \frac{1}{2} \begin{vmatrix} (1+S_l)\exp[-\mathrm{i}(k_{l+1}-k_l)x_l] & (1-S_l)\exp[-\mathrm{i}(k_{l+1}+k_l)x_l] \\ (1-S_l)\exp[+\mathrm{i}(k_{l+1}-k_l)x_l] & (1+S_l)\exp[+\mathrm{i}(k_{l+1}-k_l)x_l] \end{vmatrix} \tag{3}$$

In Eq. (3) $S_l = m_{l+1}/m_l k_{l+1}$, and the effective masses and momenta has been discretized as $m_l = m^*[(x_{l-1} + x_l)/2]$ and $k_l = k[(x_{l-1} + x_l)/2]$, respectively, x_l is the position of lth boundary.

The Fermi–Dirac distribution has been used in the tunneling current calculations of this work, and the maximum of the longitudinal electron (hole) energy was set at $20k_BT$ above (below) the bottom (top) of the conduction (valance) band, where k_B is Boltzmann constant, and T is the temperature. The trap assisted tunneling currents can calculated using Eq. (1) according to two-step tunneling: the first, from the substrate (gate) to the traps, the second, from the traps to the gate (substrate). The entire oxide/silicon interface can be assumed to be composed of many small parts (some with defects and the others without defects). And thus dilute defects can be calculated according to the following expression:

$$J = \frac{1}{s} \int_s j(x,y)\, \mathrm{d}s \tag{4}$$

where s is the area of the SiO_2 layer, $J(x, y)$ is the local tunneling current through the SiO_2 layer. In the tunneling calculations: x-grid, y-grid, and z-grid are 7, 7, and 0.1 Å, respectively.

3. Results and discussion

In the tunneling current calculations, the value of bandgap of SiO_2 8.6 eV has been used. The parameters of the effective mass and barrier height of SiO_2 have been selected according to Ref. [11] and its references: the effective electron mass has been chosen as $0.5m_0$, and the effective hole mass has been chosen as $0.38m_0$, the electron barrier height has been chosen as 3.1 eV, and the hole barrier height has been chosen as 4.4 eV. Various trap energy levels used in the tunneling current have been reported in the previous articles: 3.0 eV [4], 1.2–1.8 eV [5], 2.3 eV [6], 3.6–4.0 eV [7], 2.0 eV [8], and 2.6 eV [9]. A capture cross-section as large as 10^{-13} to 10^{-14} cm^2 for the generated acceptor like trap and a smaller capture-cross section in the region of 10^{-15} to 10^{-16} cm^2 have been reported in Ref. [3]. For simplicity, the capture cross-section of both electron and hole traps are assumed to be 4.9×10^{-15} cm^{-2} in all trap-assisted tunneling current calculations, and the inelastic tunneling is neglected.

Fig. 1 shows that the gate leakage current through the perfect and defect gate oxide in MOSFETs when the oxide thickness is 1.5 nm and the capture cross-section of electron traps is assumed to be 4.9×10^{-15} cm^{-2}. This figure has the typical characteristic of the stress-induced leakage current. It clearly illustrates how the stress-induced leakage current caused by the electron traps at the Si/SiO_2 interface changes with the trap level for the case of gate injection. A higher trap level will result in a larger leakage current for the shallow traps in the regime of direct tunneling, whereas the situation for the deep traps is complicate. J represents the total leakage current through the oxide with traps, and J_0 represents the tunneling current through the perfect oxide in this article.

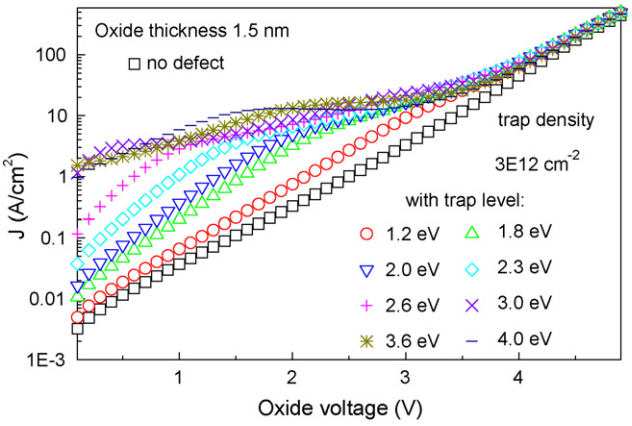

Fig. 1. The tunneling current through the oxide with the interface defects and without as a function of oxide voltage for different trap level when the electron trap density is 3.0×10^{12} cm^{-2} and locates at the transmission interface.