



Short communication

Enhancement of carrier mobility in pentacene thin-film transistor on SiO₂ by controlling the initial film growth modesQiong Qi, Aifang Yu, Peng Jiang, Chao Jiang^{*}

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ABSTRACT

Pentacene thin-film transistors (TFTs) were fabricated on thermally grown SiO₂ gate insulator under the conditions of various pre-cleaning treatments. Initial nucleation and growth of the material films on treated substrates were observed by atomic force microscope. The performance of fabricated TFT devices with different surface cleaning approaches was found to be highly related to the initial film morphologies. In contrast to the three-dimensional island-like growth mode on SiO₂ under an organic cleaning process, a layer-by-layer initial growth occurred on the SiO₂ insulator cleaned with ammonia solution, which was believed to be the origination of the excellent electrical properties of the TFT device. Field effect mobility of the TFT device could achieve as high as 1.0 cm²/Vs on the bared SiO₂/Si substrate and the on/off ratio was over 10⁶.

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1. Introduction

To realize the reliable device performance in the realistic applications, organic thin-film transistor (OTFT) needs high carrier mobility and large saturation current to be applied to the fast switch and feasible driving circuits. For this purpose, lots of approaches have been utilized to improve pentacene (C₂₂H₁₄)-based transistor's mobility, such as improving the surface roughness of the dielectric materials [1], modification the dielectric surface by self-assembled monolayer [2–7] and by optimizing the film deposition conditions [2,8,9]. Recently, several research groups report that single monolayer of pentacene with less boundary defects is virtually essential to achieve high mobility, because grain boundaries strongly affect the charge transport in pentacene films [10–12]. We also noted that, up to date, less attention was paid on the correlation between the pentacene initial growth modes and pre-cleaning treatments for the thermally oxidized SiO₂ which has been widely utilized as a dielectric layer in OTFT fabrication. In this letter, we focus on the establishment of correlation between the surface cleaning treatment and the initial pentacene film growth modes. We have found a layer-by-layer growth mode of pentacene was

established on SiO₂ under a suitable surface pre-cleaning process utilizing ammonia solution.

The mobility in saturation region can be high to reach 1 cm²/Vs and the saturated current to be 300 μA under the V_{DS} = −40 V, indicative of a promising novel pentacene thin-film transistor (TFT) fabrication approach for realistic application.

2. Experimental

The pentacene TFTs were fabricated on heavily doped n-type (0 0 1) silicon wafer having a 250 nm SiO₂ layer grown by a wet thermal oxidation process. The substrates were ultrasonically cleaned by three various approaches. Method I: cleaning with the ammonia solution NH₄OH:H₂O = 1:6, then deionized water, each for 10 min. The ammonia solution was used to etch and clean SiO₂ dielectric. Method II: cleaning with the NH₄OH:H₂O₂:H₂O = 1:1:5 (APM) and HCl:H₂O₂:H₂O = 1:1:6 (HPM), and then deionized water for 10 min, respectively. This is a traditional cleaning method used in silicon industry. The additive H₂O₂ is thought to oxidize and remove organic contaminators from the substrate, and also can protect the substrate Si from being etched by ammonia. Method III: cleaning with only organic solvents using acetone, ethanol and deionized water each for 10 min, respectively. All cleaning methods have not further introduced substrate roughness which is 0.3 nm via an AFM investigation.

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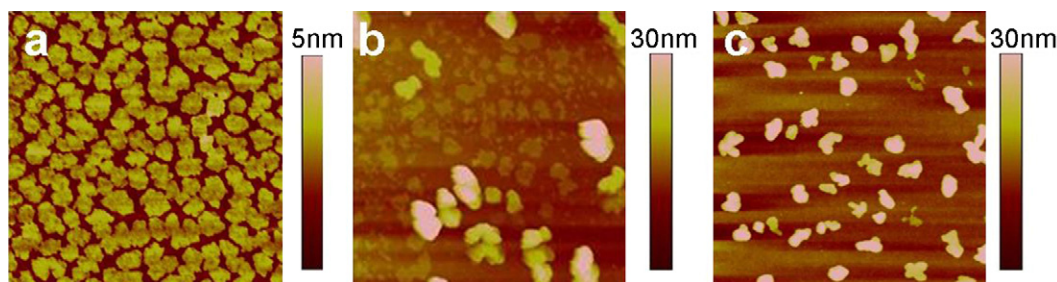


Fig. 1. $3\ \mu\text{m} \times 3\ \mu\text{m}$ AFM images of 0.5 ML pentacene film grown on SiO_2 insulator surface cleaned by (a) ammonia, (b) APM-HPM and (c) acetone and ethanol.

50 nm pentacene (Aldrich Co.) films calibrated by a quartz oscillator analyzer were deposited on the SiO_2 substrates by a commercial thermal evaporator Auto-306 (BOC-Edwards Co.) deposition system. During deposition, the back pressure reached 7×10^{-5} Pa with deposition rate 0.02 nm/s under the room temperature. Finally, 50 nm thick Au source-drain electrodes were deposited through a shadow mask onto the pentacene film at a rate of 0.4 nm/s to finish the top-contact TFTs fabrication. The conductance channel length and width were 50 and 2000 μm , respectively. The morphology of the pentacene film was characterized by a Nanoscope III (Veeco Co.) AFM using a tapping mode. The contact angle was measured using distilled water and the transfer curve of TFT was characterized using a Kethley-4200 semiconductor analyzer.

3. Results and discussion

Fig. 1 shows the AFM images of pentacene film grown on various treated SiO_2 surfaces with a nominal thickness of 0.5 monolayer (ML). On the surface treated with ammonia (Fig. 1a), pentacene molecules homogeneously nucleate and form flat islands with round-disk shapes and smooth borders. These islands connect with each other to construct a sub-monolayer with a typical height of approximately 1.5 nm, being very similar to what was ever observed under hyper thermal molecular beam deposition [9]. On the contrary, the pentacene islands are located disorderly on the substrate with different sizes, heights, and shapes on the surface treated with the acetone and the ethanol, respectively (Fig. 1c). The contact angle of the surface treated with ammonia is much smaller than that of the surface treated with acetone and ethanol (Table 1). It indicates that most of the organic contaminants on the surface of SiO_2 have been washed away by the ammonia, and a more hydrophilic surface was formed. We infer that this surface had higher surface energy, which has been demonstrated to be essential for forming large pentacene islands in the initial stages of growth [13]. When SiO_2 surface are treated with the HPM and APM (Fig. 1b), the morphology shows an intermediate situation. We inferred that the addition of H_2O_2 may reduce the cleaning efficiency of ammonia solution in two aspects. First, addition of H_2O_2 is thought to lessen the dissolving rate of SiO_2 . Second, H_2O_2 can oxidize the contaminator Si which induced during the incision process of SiO_2/Si substrate into contaminator SiO_2 , which is more difficult to be removed. A cleaner oxide surface

contains less defects and nucleation sites, and hence pentacene can possess longer migration length before the adsorbed molecules join into the boundaries and form larger islands on SiO_2 insulator, as indicated in Fig. 1a.

The rocking curves by X-ray diffraction for the three 50 nm thick pentacene films show a pure thin-film phase characterized (Fig. 2). The intensity of peak is significantly stronger on gate dielectrics cleaned with the ammonia and the APM-HPM approaches than that cleaned with the organic solvent, indicative

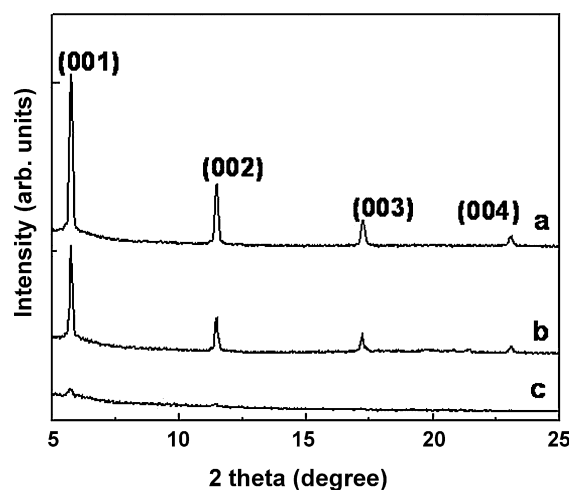


Fig. 2. XRD patterns of 50 nm thick pentacene deposited on SiO_2 insulator cleaned by (a) ammonia, (b) APM-HPM and (c) acetone and ethanol.

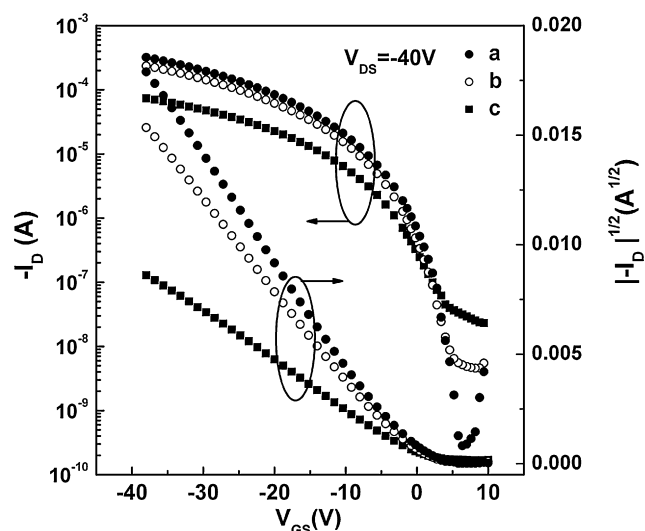


Fig. 3. Electrical-transfer characteristics of TFTs fabricated on SiO_2 insulator cleaned by (a) ammonia, (b) APM-HPM and (c) acetone and ethanol.

Table 1

Summarized properties resulting from three different surface cleaning treatments. μ is the charge carrier mobility, V_T is the threshold voltage and Θ is the water contact angle of different cleaned surfaces.

Surface treatment	μ (cm^2/Vs)	V_T (V)	$I_{\text{on}}/I_{\text{off}}$	Θ (degree)
Ammonia	1.0	-1.1	1×10^6	51
APM-HPM	0.72	-1.0	5×10^4	50
Acetone-ethanol	0.21	0.90	3×10^3	62

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