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Antireflective nanostructures fabricated by reactive ion etching method on pyramid-structured silicon surface

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ABSTRACT

In this paper, pyramid-structured silicon wafers were etched in a reactive ion etching system at room temperature and without any negative voltage pulses to obtain antireflective nanostructures. The effects of the etching time, etching power and the flow ratio of the SF_6 and O_2 (F_{SF6}/F_{O2}) on the morphologies and reflective properties of the etched samples were studied. Scanning electron microscope was used to investigate the morphologies of etched samples. The surface reflectance measurements were carried out using UV–vis–NIR spectrophotometer. A reflectance of 4.72% from the etched surface in the wavelength range of 400–800 nm was obtained under etching time of 20 min, etching power of 150 W and F_{SF6}/F_{O2} of 18 sccm/6 sccm. Meanwhile, samples etched with F_{O2} lower than 6 sccm can't get low reflective silicon structure. Besides, the results show that overlong etching time of 30 min and too big etching power of 225 W would make the nanostructures too sparse to obtain a low reflectance.

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1. Introduction

'Black silicon' is an promising anti-reflective nanostructure for silicon solar cells, which was first fabricated using femtosecond laser pulsed method by Mazur lab of Harvard University in 1998 [1]. After that, many methods were tried to get device-grade black silicon with enough size and lower down the cost [2–11], in which, reactive ion etching (RIE) technique is thought as a good solution. In 2010, average reflectance of 8.9% in 300–850 nm was obtained from the single-crystalline silicon (sc-Si) surface after being processed using RIE technique by Yoo [6]. And next, Lauri Sainiemi used cryogenic deep RIE method to fabricate silicon surface with reflectance of lower than 0.04% in the wavelength of 200–500 nm at −120 °C [7]. In 2012, reflectance of 4.2% from sc-Si surface was obtained by using RIE technology with magnetron sputtered Ag nanoparticles as the micromasks by Bi et al. [8]. At the same year, Xia used plasma immersion ion implantation method with −500 V negative voltage pulses applied to the sample stage to etch the multi-crystalline silicon and obtained uniform porous and needle-like microstructures with the average reflectance of 4.87% and 2.12%, respectively [9]. But in all of the reported RIE processes [6–9], either low temperature or great negative voltage pulses or mask was used, which are not easy ways and cost heavily. And as well known, using pyramid-structured sc-Si instead of plane one as substrate wafer can obtain lower reflectance [10,11].

In this paper, pyramid-structured sc-Si wafers were etched by a homemade RIE system using SF_6 and O_2 as etching gases without any negative voltage pulses and the whole etching process was at room temperature. The effects of the etching time, etching power and the flow ratio of the SF_6 and O_2 (F_{SF6}/F_{O2}) on the morphology and surface reflectance of sc-Si were systematically studied.

2. Experimental details

Some unpolished and (100)-oriented p-type sc-Si wafers with resistivity of 2 ± 0.05 Ωcm and thickness of 200 ± 10 μm were used to fabricate the antireflective nanostructures. All of the samples in this study were cut into 2.5 cm × 2.5 cm and then cleaned with acetone, ethanol and deionized water (DI water, >18.2 MΩ cm) in file to remove the adsorbed dust and surface contamination. After that, the silicon wafers were immersed into diluted HF solution (5 wt.%) for 15 s to remove the native oxide and rinsed in DI water. Then the wafers were etched by the sodium hydroxide solution (NaOH, 25 wt.%) to remove surface damages (∼15 μm from each

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Table 1
RIE process parameters and reflectance results of the 7 etched samples etched at 2 Pa.

Sample	Etching time (min)	Etching power (W)	F_{SF6}/F_{O2}	Reflectance (400–800 nm) (%)
1	10	75	18 sccm/6 sccm	7.31
2	10	150	18 sccm/6 sccm	5.92
3	10	225	18 sccm/6 sccm	7.96
4	10	150	18 sccm/2 sccm	22.90
5	10	150	18 sccm/4 sccm	16.75
6	20	150	18 sccm/6 sccm	4.72
7	30	150	18 sccm/6 sccm	6.86

side) caused by saw wires, which is essential in solar cells fabrication. And then the wafers were immersed into 5 wt.% HF solution for 15 s to remove the resultants (sodium silicate, etc.) generated in the damage removal process. The antireflective microstructures can be mainly prepared by the following two steps. First, the anisotropic etching was carried out in 2.5 wt.% NaOH and 5 vol.% iso-propyl alcohol mixed solution at 85 °C for 40 min to form pyramidal structures on the silicon wafer surface and then the wafers were immersed into 5 wt.% HF solution for 15 s. Next, the pyramid-structured wafers were etched in a homemade RIE system at room temperature and without any negative voltage pulses. The influences of the etching parameters on the surface morphology and antireflective property of the etched samples were systematically investigated.

The surface morphological studies of the etched samples were performed by using field emission scanning electron microscopy (FE-SEM, Hitachi, S-4800). And the surface reflectance measurements were carried out using UV–vis-NIR spectrophotometer (Shimadzu, UV-3600, with an integrating sphere) in the wavelength range of 200–1100 nm.

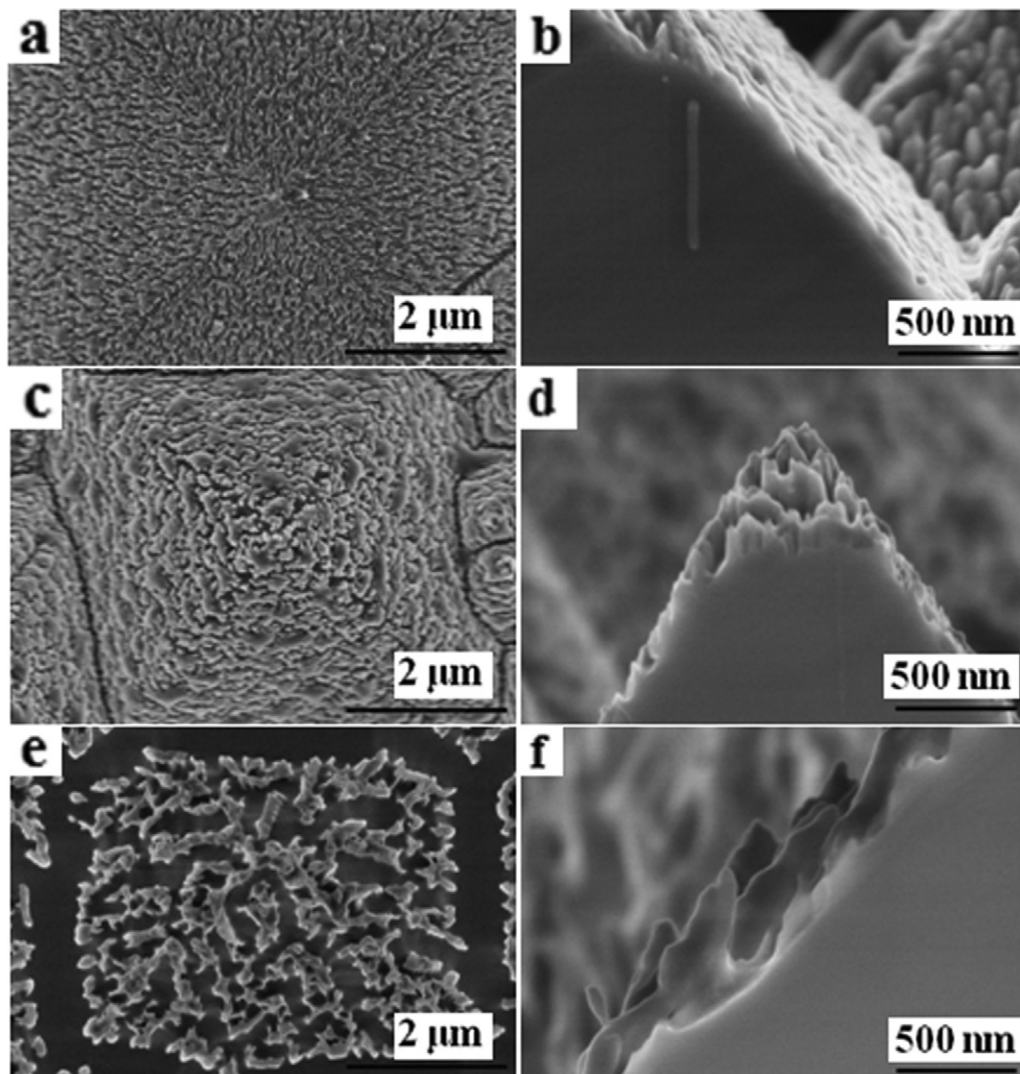

Fig. 1. SEM images of the as-etched samples with different etching power: (a) 75 W, surface; (b) 75 W, cross-section; (c) 150 W, surface; (d) 150 W, cross-section; (e) 225 W, surface; and (f) 225 W, cross-section.

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