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Microstructure and electrical characterization based on AFM of very high-doped polysilicon grains

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Abstract

In this work, we demonstrate that atomic force microscopy allows topography measurement as well as the local electrical properties of very high-doped polysilicon film prior to any subsequent annealing. AFM and TEM observations showed the columnar microstructure of the polysilicon layer. The electrical effect of this microstructure was characterized using SCM, KFM and C-AFM. Each electric mode gives additional information on the local properties of the polysilicon layer.

Keywords: ISD polysilicon; LPCVD; AFM; TEM; SCM; Surface potential; C-AFM

1. Introduction

This study was made in the context of the NXP system based on the extreme integration level of all passive components on a highly resistive silicon substrate. The passive integration technology (PICS for passive integration connective substrate) uses as upper electrode a highly doped polysilicon layer (Fig. 1) [1,2]. Good knowledge of its electrical and physical characteristics, through inquiries on doping level, grain size and doping distribution, is essential to good have a full understanding of electrical behaviors and reliability of devices [3,4].

The polysilicon takes one of the most important place in the microelectronic technology. It allows a huge malleability because of its different ways to deposit it and allows electrical behaviors close to mono-crystalline silicon [5–9].

In this context, the aim of this paper is to report microstructure and electrical characteristics of as-deposited ISD (in situ doped) polysilicon layer prior to any subsequent annealing, in an attempt to understand dopant distribution mechanisms during the deposition stage. Results on the evaluation of grain size, doping level and distribution, based on atomic force microscopy (AFM) technique including electric modes, will be presented. Microstructural characterization was also ensured through transmission electron microscopy (TEM) study.

2. Experiments details

2.1. Synthesis

In order to study ISD polysilicon layer, planar wafers without any structures. The samples are made up with a stack of various layers. The arrangement of layers is described as following (Fig. 2):

- LPCVD TEOS oxide; 1.50 μm,
- ISD polysilicon; 1.80 ± 0.1 μm; $\rho = 7$ mΩ cm,
- thin thermal oxide; 100 nm,
- substrate P-doped silicon ⟨1 0 0⟩ – 670 μm; $\rho = 1$ kΩ cm.

The in situ doped (ISD) polysilicon layer was deposited by low pressure chemical vapor deposition (LPCVD) technique synthesized in a 6 in. horizontal furnace, which technique

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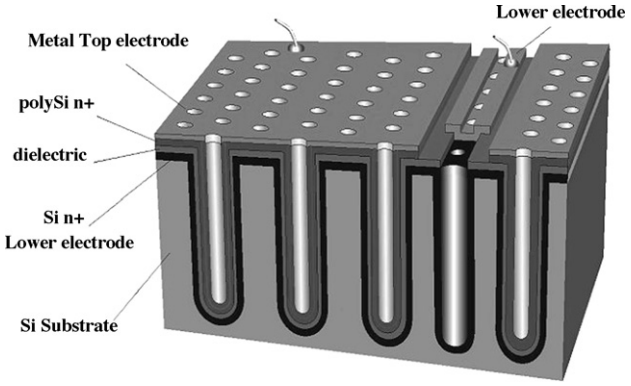

Fig. 1. PICS process.

Fig. 2. Schematic cross-section of the sample.

should ensure a more conformal polysilicon coverage for high aspect ratio structures filling (PiCS process context) [10].

The temperature and pressure conditions, $T = 635\ ^{\circ}C$ and $P = 250$ mTorr (butterfly-valve regulated) should imply a $\langle 1\ 1\ 0 \rangle$ texture, depend on pure polysilicon grains full study of Kretz [11]. Our layer is hugely doped, thanks to in situ incorporation of phosphorous during the deposition stage, by addition of a silane diluted phosphine gas according to a gamma ratio (PH_3 moles/SiH_4 moles) close to 3000 ppm.

No subsequent annealing was performed, the aim being to analyze the doping distribution inside an as-deposited polysilicon layer before phosphorous atoms migration due to annealing treatments. The expected average phosphorous doping concentration is 10^{20} atoms/cm^3. This value was found to be in good agreement with secondary ions mass spectroscopy (SIMS) and Hall analysis. The mobility value from Hall mobility measurements is about 30 cm^2/V s.

2.2. AFM and TEM conditions

For AFM imaging, samples were prepared by cleavage then the cross section was scanned. No specific surface treatment was necessary. For electrical modes, cleaved samples were mounted on a conductive holder. Ohmic contacts were achieved with silver paint.

AFM provides both surface topographical information and electrical properties at a nanometer scale. Measurements have been performed with a Dimension 3100 Atomic Force Microscope manufactured by Digital Instruments. All acquisitions were obtained at room temperature. A vibration isolation table was employed to eliminate ground vibration and acoustic noise.

First, for microstructures analysis, AFM and TEM observations were performed. For the AFM, we used the tapping mode to analyze the morphological details of ISD polysilicon layer. The tapping mode AFM is an almost non-destructive mode because it consists in an intermittent contact between the tip and the sample. A commercial monolithic silicon probe with a tip radius less than 10 nm was used. The resonant frequency of the oscillating tip was 300 kHz. For TEM observations, electron transparent thin lamella was Focused Ion Beam prepared (200 XP FEI single beam FIB) using lift-off in situ technique. TEM observations were performed in a 200 kV JEOL 2011 FEG electron microscope equipped with a high-resolution objective lens ($C_s = 1$ mm) and a GATAN tilting-rotating sample holder. To avoid layer superimposition artifact, the lamella had to be very precisely aligned with the electron beam perpendicular to whole plane, that is parallel to $\langle 1\ 1\ 0 \rangle_{Si}$ crystallographic axis of the silicon substrate.

Second, a detailed study of electric properties was done. Electrical measurements with nanometer scale resolution are very important for understanding both the transport properties and device operation mechanisms. These parameters are necessary to improve the device performance. In recent years [12], different electrical modes were developed on atomic force microscope. Since these modes are mainly devoted to detect electrical response, three electrical modes, based on AFM, were used: SCM (scanning capacitance microscopy), surface potential microscopy and conductive AFM.

SCM acquisitions provide qualitatively charge distribution in semiconductors with a spatial resolution set by the tip radius (typically 10 nm). The SCM spectroscopic mode allows measuring of local differential capacitance variation (dC/dV) versus tip voltage. The SCM probe is a commercial probe with Pt–Ir metal coated. An alternative bias voltage superimposed to a dc voltage is applied between the sample and the tip. The MIS capacitance variation is measured with a highly sensitive capacitance sensor, small as 10^{-18} F/(Hz)$^{1/2}$.

The surface potential microscopy sometimes referred as KFM (Kelvin force microscopy) maps the local variations of the surface potential of the sample.

Conductive force microscopy (C-AFM) is a current sensitive technique of conductivity variation in resistive semiconductors.

3. Results and discussion

3.1. Polysilicon topography

Extensive research has been done on Polysilicon thin films [13]. Depending on deposition conditions, the polycrystalline films can have a texture in columns or consist in a random superposition of grains of various sizes. Polysilicon material is viewed as composed of crystallites; joined together by grain boundaries [14]. Inside each crystallite, the atoms are arranged in a periodic manner so that it can be considered as a small single crystal. At the grain boundary, atoms correspond to a transitional region between different orientations of