



# Improved electrical and interfacial properties of RF-sputtered $\text{HfAlO}_x$ on n-GaAs with effective Si passivation

P.S. Das<sup>a,b,\*</sup>, A. Biswas<sup>b</sup>

<sup>a</sup> Dept. of Electronics and ECE, Indian Institute of Technology, Kharagpur 721302, India

<sup>b</sup> Institute of Radio Physics and Electronics, University of Calcutta, 92 A P C Road, Kolkata 700009, India

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## ABSTRACT

In this paper, we present the effects of ultrathin Si interfacial layer on the physical and electrical properties of GaAs MOS capacitors fabricated using RF-sputtered  $\text{HfAlO}_x$  gate dielectric. It is found that  $\text{HfAlO}_x/\text{Si}/\text{n-GaAs}$  stack exhibits excellent electrical properties with low frequency dispersion ( $\sim 4.8\%$ ), hysteresis voltage (0.27 V) and interface trap density ( $1.3 \times 10^{12} \text{ eV}^{-1} \text{ cm}^{-2}$ ). The current density of  $3.7 \times 10^{-5} \text{ A/cm}^2$  is achieved with an equivalent-oxide-thickness of 1.8 nm at  $V_{\text{FB}} + 1 \text{ V}$  for Si-passivated  $\text{HfAlO}_x$  films on n-GaAs. X-ray photoelectron spectroscopy (XPS) analysis shows that the suppression of low-k interfacial layer formation is accomplished with the introduction of ultrathin Si interface control layer (ICL). Thus the introduction of thin layer of Si between  $\text{HfAlO}_x$  dielectrics and GaAs substrate is an effective way to improve the interface quality such as low frequency dispersion, hysteresis voltage and leakage current. Additionally, current conduction mechanism has been studied and the dominant conduction mechanisms are found to be Schottky emission at low to medium electric fields and Poole–Frenkel at high fields and high temperatures under substrate injection. In case of gate injection, the main current conduction at low field is found to be the Schottky emission at high temperatures.

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## 1. Introduction

During the last decade, substrate engineering, e.g. pseudo-morphically strained-SiGe channels grown on Si substrates for p-MOSFETs and strained-Si channels on relaxed SiGe buffer layers with the graded Ge for n-MOSFETs, has been pursued to improve the carrier mobility in the channel [1]. As the complementary metal-oxide-semiconductor (CMOS) technology develops beyond 22 nm nodes, high priority has been assigned to III–V semiconductors as channel materials motivated by the need to increase the channel mobility as well as to reduce power consumption. III–V compound semiconductors offer the advantages of high electron mobilities, rich band gap engineering, and high breakdown fields and thus are likely to outperform silicon in certain metal-oxide-semiconductor (MOS) applications such as high-speed and high power devices [2,3]. However, surface oxidation occurring on the surface of III–V semiconductors can introduce a high defect density into the devices, which detrimentally affects the electrical characteristics of devices causing the Fermi level pinning [4,5]. One key challenge in the III–V technology is to identify thermodynamically stable insulators on the III–V's that give a low interfacial density

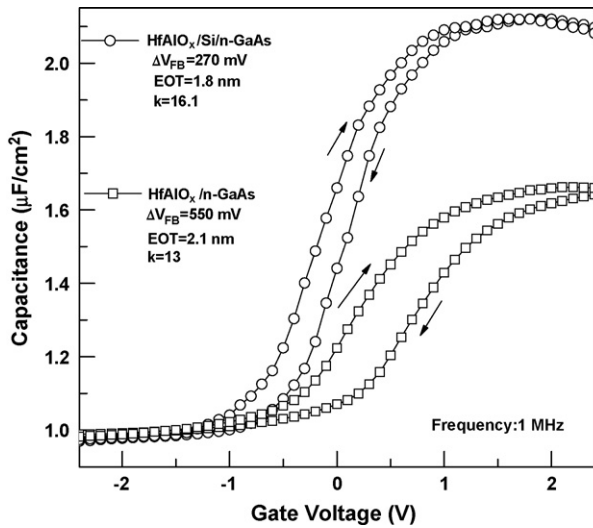
of states ( $D_{\text{it}}$ ) and a low leakage current. Among the III–V compound semiconductors, currently, GaAs is being widely studied as a potential channel material replacement of Si.

During the last decade, high-k dielectric films such as  $\text{HfO}_2$ ,  $\text{Al}_2\text{O}_3$ ,  $\text{ZrO}_2$  and  $\text{TiO}_2$  are extensively researched for their potential as substitution for  $\text{SiO}_2$ . Recently, Hf-based dielectrics have been considered as very promising high permittivity material for future gate dielectric applications. But, direct deposition of  $\text{HfO}_2$  on GaAs exhibited anomalous characteristics with large frequency dispersion, hysteresis, low effective mobility and also high leakage current [6,7]. The interfacial layer growth may be overcome by introducing interface control layers (ICLs) such as Si, Ge, and  $\text{Gd}_2\text{O}_3$  [9–11]. In addition, there have been some attempts to adopt composite films of  $\text{Al}_2\text{O}_3$  and  $\text{HfO}_2$  on GaAs substrates [8,12]. In this paper, we studied the electrical and structural properties of RF-sputter deposited  $\text{HfAlO}_x$  on n-GaAs substrates in the presence of the ultrathin silicon interface control layer. X-ray photoelectron spectroscopy (XPS) analysis was performed to investigate the interfacial properties of GaAs MOS capacitors.

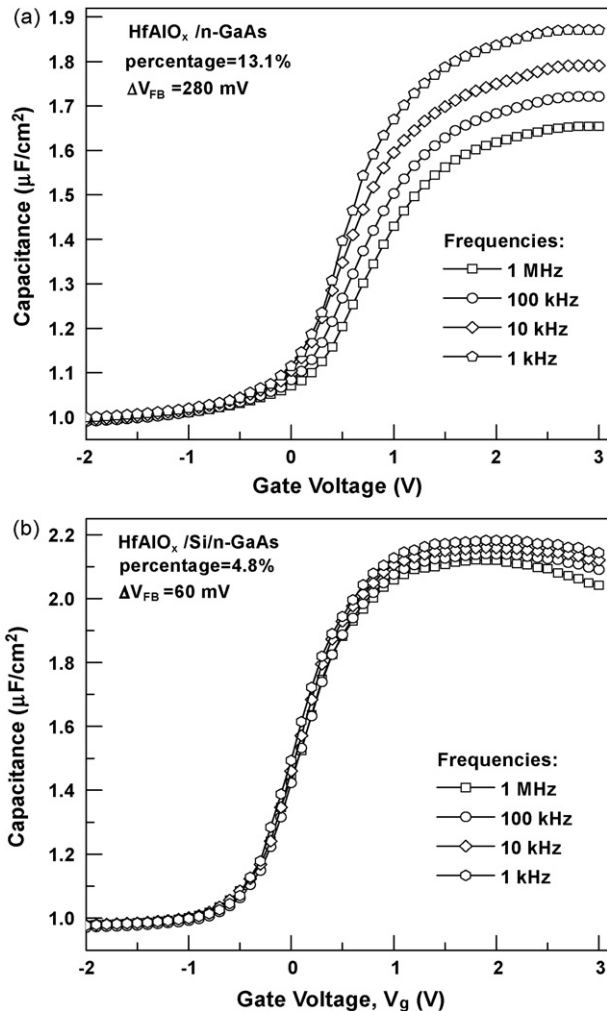
## 2. Experiments

MOS capacitors were fabricated on Te-doped n-GaAs (100) wafers with a carrier density  $\sim 1 \times 10^{16} \text{ cm}^{-3}$ . The samples were degreased in methanol, acetone and 2-propanol successively for

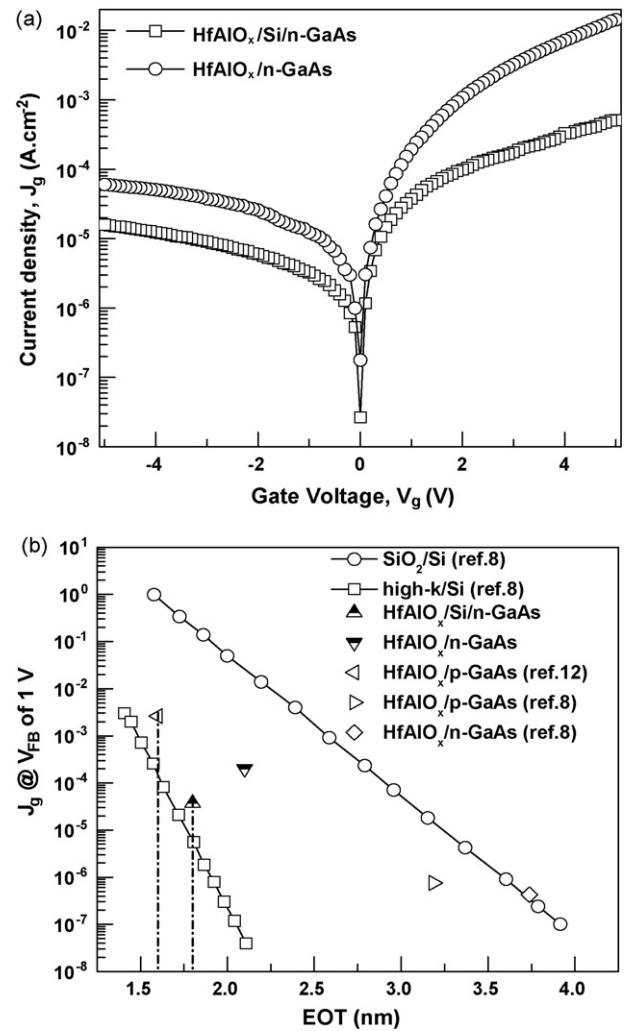
\* Corresponding author at: Dept. of Electronics and ECE, Indian Institute of Technology, Kharagpur 721302, India. Tel.: +91 3222 281475; fax: +91 3222 255303.  
E-mail address: [parthacu05@gmail.com](mailto:parthacu05@gmail.com) (P.S. Das).



**Fig. 1.** High frequency C–V characteristics of MOS capacitors on n-GaAs with S- and Si-passivation for voltage sweep from inversion to accumulation and back to inversion at a ramp rate of 0.1 V/s.



**Fig. 2.** (a) and (b) Frequency dispersion characteristics of GaAs MOS capacitors with S- and Si-passivation.



**Fig. 3.** (a) Current density versus applied bias plot ( $J$ – $V$  characteristics) of  $\text{HfAlO}_x$  thin film on n-GaAs with S- and Si-passivation and (b) gate leakage current density at  $V_{\text{FB}} \pm 1$  V versus EOT. For comparison, reported data of high- $k$  on Si,  $\text{SiO}_2$  on Si,  $\text{HfAlO}_x$  thin films on GaAs are also plotted together.

2 min each. Then the substrates were treated with 50% HCl for 5 min and heated in  $\text{NH}_4\text{OH}$  at  $60^\circ\text{C}$  for 10 min to remove native oxide. After wet chemical cleaning, the samples were heated into 40% ammonium sulfide solution for 10 min for S-passivation of GaAs surface. The  $\text{HfAlO}_x$  films were deposited at  $50^\circ\text{C}$  by RF co-sputtering of  $\text{Al}_2\text{O}_3$  and  $\text{HfO}_2$  targets in 100W powers in Ar atmosphere at  $10^{-3}$  mbar working pressure. Prior to the dielectric deposition, ultrathin silicon layer of 1.5 nm was deposited as interface control layer (ICL) on some of the samples by RF sputtering in the same ambient. Thickness of the dielectric layer was measured to be  $\sim 7$  nm using an ellipsometer. The post deposition annealing (PDA) was carried out in an  $\text{N}_2$  ambient at  $600^\circ\text{C}$  for 1 min by rapid thermal annealing. Finally, Al electrode was formed by thermal evaporation with the gate area of  $1.96 \times 10^{-3} \text{ cm}^2$  at  $10^{-6}$  mbar using the shadow masking technique. In order to make the backside ohmic contact Au/Ge/Au was deposited at a pressure of  $10^{-6}$  mbar. For chemical analysis, high-resolution XPS was performed using VG ESCALAB 220i-XL system. Capacitance–voltage (C–V) measurements were made using Agilent E4980A LCR meter and current–voltage ( $I$ – $V$ ) measurements were performed with HP4156C semiconductor parameter analyzer, respectively.

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