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Influence of surface cleaning effects on properties of Schottky diodes on 4H–SiC

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ABSTRACT

Ir/4H–SiC and IrO_2/4H–SiC Schottky diodes are reported in terms of different methods of surface pretreatment before contact deposition. In order to find the effect of surface preparation processes on Schottky characteristics the SiC wafers were respectively cleaned using the following processes: (1) RCA method followed by buffered HF dip. Next, the surface was oxidized (5.5 nm oxide) using a rapid thermal processing reactor chamber and circular geometry windows were opened in the oxide layer before metallization deposition; (2) the same as sequence (1) but with an additional *in situ* sputter etching step before metallization deposition; (3) cleaning in organic solvents followed by buffered HF dip. The *I–V* characteristics of Schottky diodes were analyzed to find a correlation between extracted parameters and surface treatment. The best results were obtained for the sequence (1) taking into account theoretical value of Schottky barrier height. The contacts showed excellent Schottky behavior with ideality factors below 1.08 and barrier heights of 1.46 eV and 1.64 eV for Ir and IrO_2, respectively. Very promising results were obtained for samples prepared using the sequence (2) taking into account the total static power losses because the modified surface preparation results in a decrease in the forward voltage drop and reverse leakage current simultaneously. The contacts with ideality factor below 1.09 and barrier height of 1.02 eV were fabricated for Ir/4H–SiC diodes in sequence (2).

1. Introduction

Silicon carbide metal/semiconductor devices are rapidly growing in importance because of issues currently surrounding the performance of SiC-based metal/oxide/semiconductor field-effect transistors (MOSFETs). An advantage of SiC is that it can be thermally oxidized to form a SiO_2/SiC structure. However, in spite of more than 20 years of research, difficulties surrounding thermal oxidation of SiC surfaces have not yet been overcome and MOSFETs are not yet commercially available. The main reason for this is the low value of inversion channel mobility which is still far below the predicted value for bulk SiC [1,2]. Despite these issues, SiC MOSFETs are still promising candidates for high-power electronic devices.

The limited quality of SiC wafers has caused that very important processes of surface cleaning and initial preparation are almost totally baffling. The high density of crystal imperfections like micropipes and dislocations seems to be affecting the device properties stronger than the results of cleaning and surface preparation. Currently, further progress in the surface modification will be required to solve the problem of low inversion channel mobility and device capability. The research progress is following a very similar trend to be observed for silicon technology.

In this study, in order to find a suitable conditions of surface preparation, we applied various surface treatment based on (1) RCA method, (2) RCA method enhanced by non-reactive *in situ* sputter etching and (3) cleaning in organic solvents followed by buffered HF (HF_{buff}) dip. Ir/4H–SiC and IrO_2/4H–SiC Schottky diodes were fabricated to ascertain the efficiency of the cleaning processes on Schottky contact performance.

The rare earth metal and its oxide were mainly used because the Schottky barrier height values of widely investigated metals with high work functions (Ni, Pt, Au and Pd) were lower than those predicted by the Schottky–Mott theory [3–5]. Additionally, most of the metals interdiffuses into SiC within the temperature range of 450–500 °C leading to instability of Schottky barrier height [6–8]. The abovementioned problems could be overcome by application of the rare earth metals and their conducting oxides which have higher work function (Ir: 5.6 eV and IrO_2: 5.8 eV) and create more

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thermally stable metal/semiconductor interface [9,10]. The kinetic of formation of iridium silicides is controlled by diffusion of silicon species through the incipient layer of silicide. One of the latest analysis of iridium silicide formation on silicon shows that the interval of complete silicidation ranges between 450 °C and 530 °C [11]. It suggests that the transition temperature is higher on silicon carbide and iridium is a very promising Schottky barrier material for high temperature electronics. Synchrotron radiation photoemission spectroscopy (SRPES) shows that the work function of IrO_2 is higher about 0.23 eV than that of Ir what leads to additional increase of Schottky barrier height [12]. Simultaneously, the barrier height of IrO_2/4H–SiC contact increases after annealing as a result of Si outdiffusion to the IrO_2 film. In such a case the Schottky barrier height is not only determined by the bulk properties of metal and semiconductor. The interface properties, such as the metal-induced gap states (MIGS) and interface defects influence on the Schottky barrier height [13]. In particular, many factors may affect Schottky barrier height in rectifying contacts on SiC. Majority of the factors concerns the control of the surface preparation prior to metal deposition. Indeed, the electrical behavior of Schottky contact has been observed to be strongly dependent on the quality of the metal/semiconductor interface [14,15]. It was shown that the interface quality could be improved by RTP annealing of Ni/6H–SiC contacts as a result of silicide formation while a silicon carbide layer is consumed by the solid-state reaction. Then, the consumption of the SiC layer leads to the removal of surface damages while contaminations are embedded in the silicide [16]. In this work, the *I–V* characteristics were analyzed to find a correlation between extracted parameters of Ir/4H–SiC and IrO_2/4H–SiC Schottky diodes and initial surface treatment.

2. Experimental

Ir/4H–SiC and IrO_2/4H–SiC Schottky diodes were fabricated on n^+-type substrates with an n-type epitaxial layer from Cree Research Inc. The effective doping density of the epitaxial layer was 5×10^{15} cm^{-3}. In order to find the effect of surface preparation process on Schottky characteristics the wafers were respectively cleaned using the following processes:

(1) organic solvents (trichloroethylene, acetone and propanol) and sequentially etching in boiling NH_4OH–H_2O_2–H_2O (1:1:5) and HCl–H_2O_2–H_2O (1:1:5) solutions for 10 min (RCA clean) and HF_{buff} dip for 30 s followed by rapid thermal oxidation (RTO) at 1100 °C for 10 min. The circular geometry windows were opened in the thermal oxide layer after backside contacts fabrication and prior to Schottky metal deposition;
(2) sequence (1) enhanced by non-reactive *in situ* sputter etching by argon ions for 40 s in opened windows area;
(3) organic solvents (trichloroethylene, acetone and propanol) and HF_{buff} dip for 3 min.

Backside ohmic contacts were formed by dc magnetron sputtering deposition of 200-nm thick Ni film. Prior to contact deposition, top surface was protected by photoresist while the backside oxide film was etched in HF_{buff}. The rapid thermal annealing (RTA) process was carried out at 950 °C in Ar for 3 min to decrease the ohmic contacts resistivity. Circular Ir and IrO_2 Schottky contacts were formed on epitaxial layer by lift-off photolithography. 50-nm thick Ir film was deposited by dc magnetron sputtering from Ir target in Ar (P_{DC} = 50 W, $p_{Ar} = 1 \times 10^{-2}$ mbar). Thin films of iridium oxide (50-nm thick) were fabricated by RF reactive magnetron sputtering from Ir target in O_2/Ar plasma at oxygen to argon pressure ratio of 0.1. The static *I–V* characteristics of Schottky contacts were measured using Keithley 251 Source Meter. Three methods were applied to extract Schottky barrier height (SBH) from forward *I–V* characteristics (proposed by Rhoderick and Williams [17], Cheung and Cheung [18] and Norde [19]).

3. Results and discussion

The forward and reverse current density versus voltage measured at room temperature is shown in Figs. 1 and 2, respectively. The forward current density is linear over more than four orders of magnitude at low voltages for every diode. The linearity of the characteristic for selected Ir/4H–SiC diodes is even more than nine orders of magnitude. It confirms very strong influence of the applied method of surface preparation on diode properties. The current density tends to saturate at higher voltages due to the series resistance of the diode.

Schottky barrier height φ_b, ideality factor η and specific resistance R_{sp_ON} of the diodes were extracted from *I–V* measurements using three different methods which are based on thermionic emission theory. According to the mentioned theory the *I–V* relationship for Schottky junction is given by the following equation:

$$I = A^{**}AT^2 \exp\left(-\frac{q\phi_{b_0}}{kT}\right)\left(\exp\frac{qV}{\eta kT} - 1\right) \quad (1)$$

where A^{**} is the effective Richardson constant, A is diode area, ϕ_{b_0} is apparent barrier height at zero-bias while η is ideality factor. For our calculations the theoretical value of A^{**} was used for 4H–SiC (146 A cm^{-2} K^{-2}) [20] which was determined by using a value of the effective mass of 0.2 m_0 [21]. The voltage (V) in Eq. (1) is often

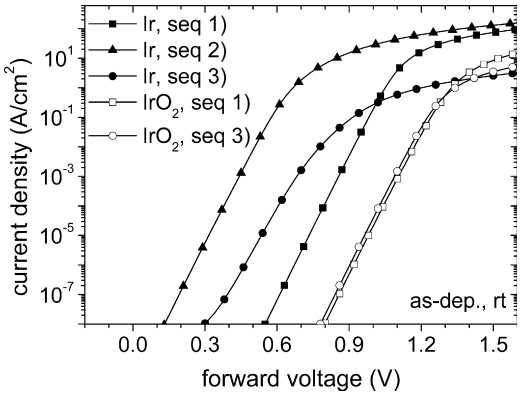

Fig. 1. Forward *J–V* characteristics of as-deposited Ir/4H–SiC and IrO_2/4H–SiC diodes at room temperature.

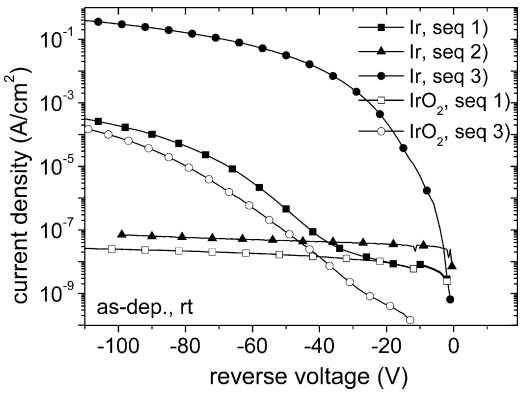

Fig. 2. Reverse *J–V* characteristics of as-deposited Ir/4H–SiC and IrO_2/4H–SiC diodes at room temperature.