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Characterization of Y_2O_3 gate dielectric on n-GaAs substrates

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ABSTRACT

Physical and electrical properties of sputtered deposited Y_2O_3 films on NH_4OH treated n-GaAs substrate are investigated. The as-deposited films and interfacial layer formation have been analyzed by using X-ray photoelectron spectroscopy (XPS) and secondary ion mass spectroscopy (SIMS). It is found that directly deposited Y_2O_3 on n-GaAs exhibits excellent electrical properties with low frequency dispersion (<5%), hysteresis voltage (0.24 V), and interface trap density (3×10^{12} eV^{-1} cm^{-2}). The results show that the deposition of Y_2O_3 on n-GaAs can be an effective way to improve the interface quality by the suppression on native oxides formation, especially arsenic oxide which causes Fermi level pinning at high-*k*/GaAs interface. The Al/Y_2O_3/n-GaAs stack with an equivalent oxide thickness (EOT) of 2.1 nm shows a leakage current density of 3.6×10^{-6} A cm^{-2} at a V_{FB} of 1 V. While the low-field leakage current conduction mechanism has been found to be dominated by the Schottky emission, Poole–Frenkel emission takes over at high electric fields. The energy band alignment of Y_2O_3 films on n-GaAs substrate is extracted from detailed XPS measurements. The valence and conduction band offsets at Y_2O_3/n-GaAs interfaces are found to be 2.14 and 2.21 eV, respectively.

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1. Introduction

The ever increasing need for higher speed and lower power consumption has already pushed the Si-based MOSFET to its performance limit. Alternative channel materials with high carrier mobility such as III–V compound semiconductors and Ge are being actively researched to supplement the device down scaling. Currently, GaAs is being considered as a potential channel material for its high carrier mobility, high breakdown strength and large band gap compared to Si [1–4]. However, unlike Si, it is difficult to achieve a stable gate insulator on GaAs by thermal oxidation. Also the native oxides on GaAs are found to induce high density of interface traps that causes Fermi level pinning [5]. Fortunately, recent development in high-*k* dielectrics allows one to explore the development of complementary metal–oxide–semiconductor (CMOS) devices using GaAs as the channel material [6–11]. The chemical or physical deposition of high-*k* gate dielectrics on bulk-GaAs, rather than thermal growth, makes them viable as insulators on GaAs substrates. Recently, some progress has been made to form gate dielectrics on GaAs substrates [11–14].

However, implementation of suitable high quality gate dielectrics is a challenging task for surface channel devices with GaAs as the channel material. Among the different high-*k* dielectrics, hafnium oxide is a very promising high permittivity material for gate dielectric applications with III–V channel materials. However, direct deposition of HfO_2 on GaAs showed abnormal capacitance–voltage characteristics with no accumulation region, large frequency dispersion, and large hysteresis voltage, which are attributed to the native oxides induced interface pinning between GaAs substrates and HfO_2 layer [11,13–15]. For gate dielectric applications, the films must satisfy two basic criteria; sufficient band offset over 1 eV to act as a barrier for both electrons and holes to reduce the leakage current and be stable in contact with the GaAs.

Yttrium oxide (Y_2O_3) is also a promising high-*k* gate dielectric as it has a moderately high dielectric constant (~16), relatively high band offsets, and exhibits a high thermodynamic stability [16]. Moreover, Y_2O_3 is one of the few high-*k* dielectrics that has a lattice constant (10.62 Å) which is almost twice that of GaAs (5.65 Å) and may result in a sharp Y_2O_3/GaAs interface with a possibility of low interface trap density. Recently, Yang et al. [17] have reported the dielectric constant in cubic HfO_2 doped with Y_2O_3 epitaxial films on GaAs showing the potential of Y_2O_3 as gate oxide. GaAs MOS devices with Y_2O_3 as a gate dielectric have not been reported yet.

In order to study the suitability of using Y_2O_3 as a possible gate dielectric in GaAs system, its interfacial properties and energy band alignment with GaAs, conduction band offset (CBO) and valence band offset (VBO) should be accurately known. In this paper, we present the results of our study on the structural and

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electrical properties of the Y_2O_3 gate stack on n-GaAs substrates. The interface properties and band alignment at Y_2O_3/n-GaAs interfaces are studied by using X-ray photoelectron spectroscopy, secondary ion mass spectroscopy, and from the electrical measurements.

2. Experiments

MOS capacitors were fabricated on n-GaAs (1 0 0) wafers. The wafers are uniformly Te doped having a carrier density of $\sim 1 \times 10^{16}\,cm^{-3}$. The wafers were degreased using methanol, acetone and 2-isopropanol for 2 min each. Then the substrates are treated with 50% HCl for 5 min and heated in NH_4OH at 60 °C for 10 min to remove the native oxide and elemental As from the GaAs surface. The Y_2O_3 dielectric layers were deposited at room temperature by RF sputter using Y_2O_3 target at 100 W RF power in an Ar ambient. The thickness of the dielectric layer was measured using Gaertner Model 365AK ellipsometer and was found to be 9.0 nm. The refractive index of deposited Y_2O_3 is found to be 1.95. Al top electrode was formed by thermal evaporation at 10^{-6} mbar with a gate area of $1.96 \times 10^{-3}\,cm^2$ using shadow masking technique. Low resistance back ohmic contact was made by using Au/Ge/Au alloy. For chemical analysis, high resolution XPS was performed using VG ESCALAB 220i-XL system. Capacitance–voltage (*C–V*) measurements were performed using Agilent E4980A LCR meter and current–voltage (*I–V*) measurements were performed with HP4156C semiconductor parameter analyzer, respectively.

3. Results and discussion

3.1. Interfacial characteristics

Fig. 1(a) shows the high frequency (1 MHz) capacitance–voltage characteristics of MOS capacitors with sputtered Y_2O_3 gate dielectric (9 nm) and Al metal gate. The dielectric constant (ε) and equivalent oxide thickness (EOT) were calculated from accumulation capacitance. The average value of dielectric constant ($\varepsilon = C_{acc}d_{Y_2O_3}/\varepsilon_0 A$) and equivalent oxide thickness ($EOT = \varepsilon\varepsilon_0 A/C_{acc}$) where, ε_0 the permittivity in vacuum, C_{acc}/A the accumulation capacitance per unit area and $d_{Y_2O_3}$ the thickness of the Y_2O_3 film, were found to be 16.4 and 2.1 nm, respectively. The flat band voltage (V_{FB}) of the MOS capacitors determined from *C–V* measurements is −0.32 V. The presence of accumulation and depletion regimes in the *C–V* characteristics of MOS capacitors with Y_2O_3 gate dielectric on n-GaAs indicates that the Fermi level is unpinned [18,19]. However, the *C–V* curves "stretch out" along the voltage axis; indicating the presence of interface trap density for directly deposited Y_2O_3 on n-GaAs substrates. The interface state density (D_{it}) is evaluated from the HF *C–V* characteristics using method proposed by Terman [20] and the extracted D_{it} is plotted as a function of energy is shown in the inset in Fig. 1(a). The minimum value of D_{it} is $\sim 3 \times 10^{12}\,eV^{-1}\,cm^{-2}$ for Y_2O_3/n-GaAs gate stack. The value is in good agreement with the reported results [21,22]. The above results indicate that Y_2O_3 can be used as a passivation layer for III–V semiconductors. In addition, the hysteresis voltage which is mainly caused by the presence of elemental As in the oxide [14,23,24] is significantly low for Y_2O_3/n-GaAs gate stacks. Hysteresis voltage is found to be 240 mV for Y_2O_3/n-GaAs stacks as shown in Fig. 1(b), is in good agreement with the high-*k* dielectrics deposited on GaAs with an interfacial passivation layer. The smaller hysteresis voltage for Y_2O_3/n-GaAs also indicates less charge trapping.

Kim et al. [21] have reported a hysteresis voltage from the devices with thicker HfO_2 (10 nm) and Ge interfacial layer as ∼600 mV, whereas a smaller hysteresis voltage of ∼240 mV is observed for MOS capacitors with Y_2O_3/n-GaAs gate stacks. It is worth noting that although the Y_2O_3 is directly deposited on n-GaAs in this study, the hysteresis voltage is significantly low and is comparable with high-*k* on p-GaAs with interfacial passivation layer. The results suggest that a thin film of Y_2O_3 may be used as interfacial passivation layer on III–V substrates prior to HfO_2 deposition. Although the hysteresis voltage for Y_2O_3 is low; however, it is still high compared with high-*k*/Si gate stacks, which suggests the further optimization of Y_2O_3 gate stack on n-GaAs is necessary. The boarder traps density calculated from hysteresis voltage was found to be $2.7 \times 10^{12}\,cm^{-2}$. The corresponding border trap charge density (Q_{bt}) is $4.3 \times 10^{-7}\,C\,cm^{-2}$. The values of D_{it} and N_{bt} also suggest a good interface between Y_2O_3 film and the n-GaAs substrate.

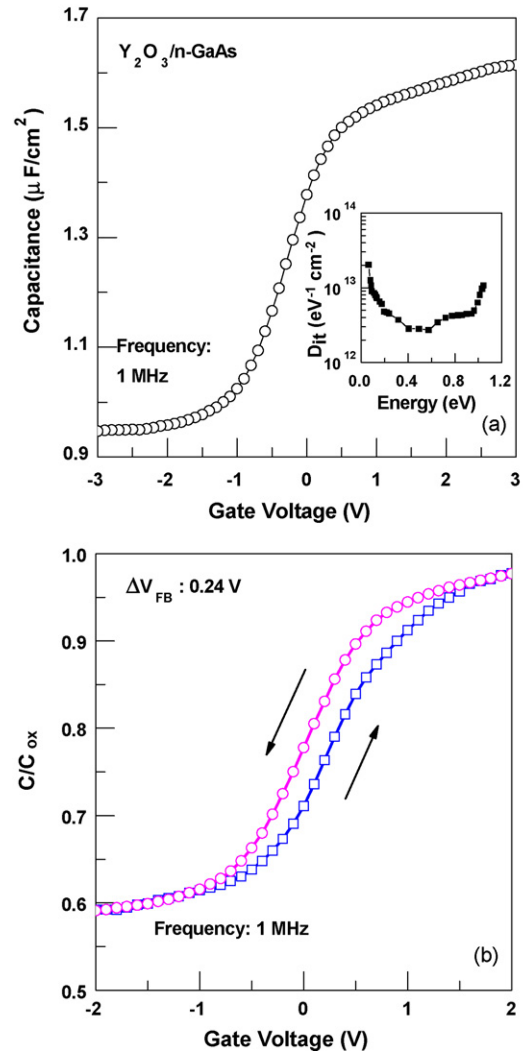

Fig. 1. (a) High frequency (1 MHz) *C–V* characteristic of MOS capacitor with 9 nm Y_2O_3 thin film on n-GaAs substrate. Inset (a) shows distribution of interface state density (D_{it}) as a function of energy ($E_c - E_t$) for GaAs MOS capacitor. (b) The hysteresis characteristic for the same gate stack.

The *C–V* characteristics measured at frequencies of 1 kHz, 500 kHz, and 1 MHz for Al/Y_2O_3/n-GaAs gate stack show frequency dispersions in both the accumulation and depletion regions and is shown in Fig. 2. The amount of frequency dispersion in accumulation capacitance, evaluated as (ΔC_{ox}) between 1 kHz and 1 MHz is 4% for the Y_2O_3/n-GaAs gate stack. The result is comparable with the high-*k* dielectrics deposited on p-GaAs substrates with an interfacial passivation layer. For any high-*k*/n-GaAs gate stack, the frequency dispersion is higher compared with

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