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Effect of erbium interlayer on nickel silicide formation on Si(1 0 0)

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Abstract

To reveal the influence of erbium interlayer on the formation of nickel silicide and its contact properties on Si substrate, Er(0.5–3.0 nm) and Ni(20 nm) are successively deposited onto Si(1 0 0) substrate and are treated by rapid thermal annealing in pure N_2 ambient. The NiSi formation temperature is found to increase depending on the Er interlayer thickness. The formation temperature of $NiSi_2$ (700 °C) is not influenced by Er addition. But with 2 nm Er interlayer, the formed $NiSi_2$ is observed textured with preferred orientation of (1 0 0). During the formation of NiSi, Er segregates to the surface and little Er remains at the NiSi/Si(1 0 0) interface. Therefore, the Schottky barrier height of the formed NiSi/n-Si(1 0 0) contact is measured to be 0.635 ~ 0.665 eV which is nearly invariable with different Er addition.

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Keywords: Ni-silicide; Er interlayer; Schottky barrier

1. Introduction

Silicides are widely used in VLSI circuits as source/drain contact materials for many years. Study of nickel silicide (NiSi) aroused much attention since it was regarded as a substitute of $CoSi_2$ for 65 nm CMOS and beyond. NiSi has many advantages, such as low resistivity, low thermal budget, and low ratio of Si consumption by Ni when formed [1,2].

NiSi has an Schottky barrier height (SBH) of 0.65 eV on n-type Si [3]. To improve the phase thermal stability of NiSi, a small amount of Pt was added to the NiSi film [2,4]. And as Pt is added, the Schottky barrier is increased to 0.71–0.73 eV because PtSi has a very high SBH (~0.8 eV) on n-type Si [5,6]. CMOS devices will be continuously scaling in future. As predicted by International Technology Roadmap for Semiconductors, the specific contact resistance of silicide with source and drain has to be reduced to $\sim 10^{-8}\ \Omega\ cm^2$ range for 65 nm technology node and beyond. The contact resistance is strongly dependent on the SBH and the surface doping level. So for the extension of NiSi application in ultra small devices, a low Schottky barrier of Ni-based silicide on n-type Si is needed.

As a comparison, rare earth silicides, such as $ErSi_{2-x}$, $YbSi_{2-x}$, etc., have a very low SBH of 0.3–0.4 eV on n-type Si [7,8]. And adding Yb to NiSi has been proved to modify the effective work function of NiSi from 4.72 to 4.22 eV in fully silicided metal-gate application [9]. Yb piling-up at the NiSi/SiON interface after silicidation annealing was shown to be the reason for the work function modulation effect. Similarly, one would expect that if Er is added to NiSi, the SBH of NiSi/n-Si(1 0 0) may be changed because of the work function modulation.

In our work, Er as an initial interlayer is added to the Ni/Si(1 0 0) structure. Formation of NiSi and Ni disilicide ($NiSi_2$) phases and the SBH of the formed NiSi on n-type Si are studied to show the influence of Er addition.

2. Experimental

N-type Si(1 0 0) wafers were used in this work. For sample preparation, the wafers, after standard RCA cleaning, were dipped in a dilute HF solution to remove residual surface oxide. After drying, they were immediately loaded into the vacuum chamber of an ion beam sputtering system. The base pressure of the chamber is better than 9×10^{-5} Pa. Er and Ni were then successively deposited onto the wafers at a pressure of 5×10^{-3} Pa in argon atmosphere. The thickness of Ni was

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kept to 20 nm while the thickness of the Er varies from 0.5 to 3.0 nm. Pure 20 nm thick Ni without Er interlayer is also deposited for a systematic study. Rapid thermal annealing (RTA) was performed at 250–900 °C for 60 s in N_2 ambient.

NiSi/n-Si(1 0 0) diodes were fabricated on oxide patterned wafer with 780 μm × 780 μm contact holes surrounded by B-doped guard rings. After metal deposition and 550 °C RTA, the patterned wafers were selectively etched in a boiling H_2SO_4:H_2O_2 solution to remove the unreacted metals.

Phase identification of the film was performed by X-ray diffractometry (XRD, D/max 2550V) with Cu Kα radiation. Atomic redistribution after RTA was investigated by Auger electron spectroscopy (AES, Microlab 310F) and secondary ion mass spectroscopy (SIMS, CAMECA IMS 6F). AES measurement was carried out with electron beam of 3 keV and a beam current of 0.47 μA. The lateral resolution of the AES is around 45 nm. Current–voltage (*I–V*) measurement was performed on the NiSi/n-Si(1 0 0) diodes with different Er addition to show the influence of Er on the NiSi/n-Si(1 0 0) contact properties.

3. Results and discussion

It is well established that the reaction of Ni with Si substrate exhibits the Ni-rich silicides–NiSi–$NiSi_2$ sequence as the annealing temperature is increased [1,2]. Among all the Ni-silicide phases, NiSi has the lowest resistivity of ~14 μΩ cm and is considered to be the best candidate for 65 nm CMOS and beyond.

Fig. 1 shows the sheet resistance of the Ni(20 nm)/Er/Si(1 0 0) samples after RTA at different temperatures. XRD scanning in Figs. 2–4 was performed on exactly the same samples for the sheet resistance measurement shown in Fig. 1. Fig. 2 shows the XRD spectra for the Ni(20 nm)/Er(2 nm)/Si(1 0 0) samples after annealing at different temperatures. And Fig. 3 shows the extra XRD spectra for the same samples but scanned in 63–71° range. The XRD spectra for the Ni(20 nm)/Si(1 0 0) samples are shown in Fig. 4.

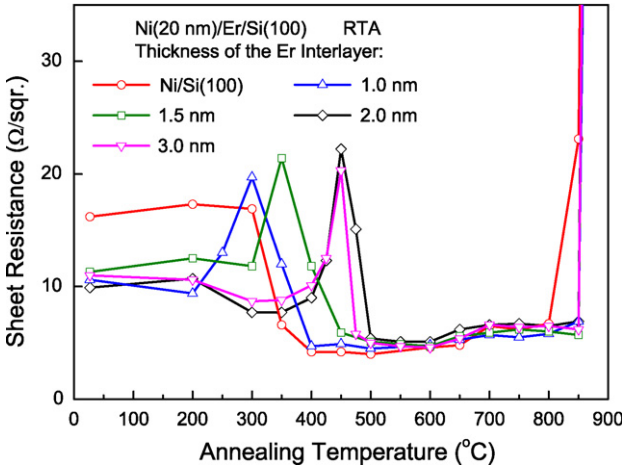

Fig. 1. Sheet resistance of the Ni(20 nm)/Er/Si(1 0 0) samples after annealing at different temperatures. The thickness of the Er interlayer varies from 0 to 3.0 nm.

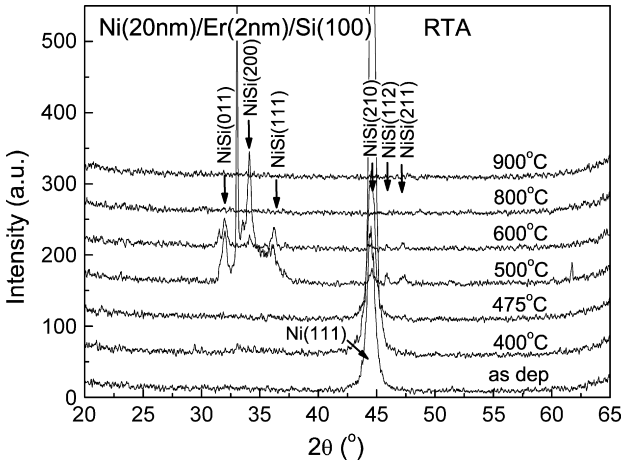

Fig. 2. XRD spectra scanned from 20 to 65° for the Ni(20 nm)/Er(2 nm)/Si(1 0 0) samples after annealing at different temperatures.

By comparing among Figs. 1–4, the most distinct observation is the shift of NiSi formation temperature. For the Ni(20 nm)/Si(1 0 0) sample, a sudden drop of sheet resistance in 300–400 °C annealing temperature range is ascribed to the phase transformation from Ni-rich silicides to NiSi since NiSi has the lowest resistivity (Fig. 1). At 400 °C annealing, NiSi is completely formed. As Er interlayer is added to Ni/Si system, the rapid drop in sheet resistance curve is shifted to higher temperature which indicates an increase in NiSi formation temperature. For the Ni(20 nm)/Er/Si(1 0 0) sample with 2.0 or 3.0 nm thick Er interlayer, NiSi is found fully formed after 500 °C annealing. Another observation is the increase in sheet resistance for the Er-added samples annealed at low temperatures just before the formation of the detectable NiSi phase. For these high-resistance samples, oxygen diffusion from the annealing ambient to the Er/Ni layer and slight mixing of the Ni, Er and Si atoms near the interface are observed by AES (not shown). The oxygen incorporation is probably caused by the high reactivity of Er to oxygen.

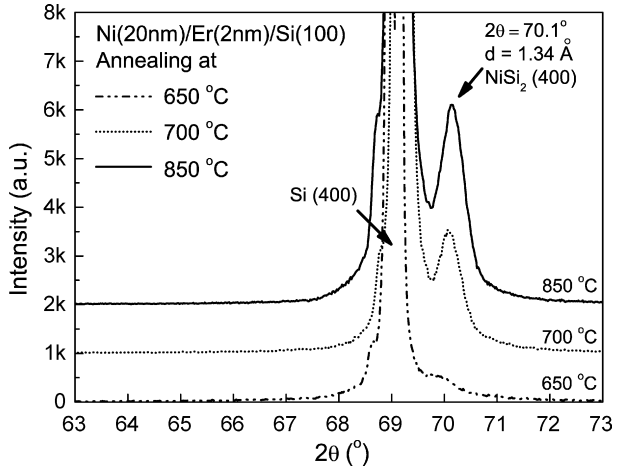

Fig. 3. XRD spectra scanned from 63 to 73° for the Ni(20 nm)/Er(2 nm)/Si(1 0 0) samples after annealing at 650, 700, and 850 °C.