Applied Surface Science 255 (2009) 7743–7748

Contents lists available at ScienceDirect

Applied Surface Science

journal homepage: www.elsevier.com/locate/apsusc

Fabrication of high Ge content SiGe-on-insulator with low dislocation density by modified Ge condensation

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ARTICLE INFO

Article history:
Received 12 November 2008
Received in revised form 22 April 2009
Accepted 24 April 2009
Available online 3 May 2009

PACS:
68.35.Fx
81.65.Mq
66.30.−h

Keywords:
Diffusion
Oxidation
Germanium silicon alloys
Semiconducting materials

ABSTRACT

A SiGe-on-insulator (SGOI) structure with high Ge content and low density of dislocations is fabricated by a modified Ge condensation technique. The formation and elimination of stacking faults during condensation process are analyzed by transmission electron microscopy. A $Si_{0.19}Ge_{0.81}OI$ substrate is fabricated utilizing two steps of oxidation and intermittent annealing. The time of oxidation or annealing at 900 °C is essential for the elimination of stacking faults in high Ge content SGOI substrate. The surface morphology of SGOI is investigated by atomic force microscopy and the defect density is evaluated from wet etching method. After the final condensation, the surface root-mean-square roughness (rms) of SiGe layer is kept below 1 nm and the threading defect density is controlled around 10^4 cm^{-2}. The smooth surface and integrated lattice structure of SiGe layer indicate that the SGOI is suitable for heteroepitaxial growth of strained Ge, GaAs and III–V compounds.

1. Introduction

SiGe-on-insulator (SGOI) is a typical template substrate for strained silicon epitaxy. The tensile strained Si and compressively strained SiGe are promising substrates for high performance metal-oxide-semiconductor field-effect transistors (MOSFETs) because they can offer higher carrier mobilities [1–3]. Recently, germanium-on-insulator (GeOI), which combines the high mobility of carriers with the advantages of SOI structure, has also been proposed as a potential engineered substrate for next-generation semiconductor technology [2,4–6]. A hole mobility of 2700 cm^2/Vs at room temperature has also been reported in a strained Ge channel [7]. If GeOI CMOS becomes the choice of technology, how to create a high quality single-crystal Ge layer on the insulator is the biggest challenge. Now there are two methods, one efficient way is offered by Smart-cut technology [2], the other is heteroepitaxial growth of Ge on high Ge content SGOI substrate [5]. Actually, the later process is more attractive because it seems to be more suitable for large diameter wafers (over 200 mm). Thus, it is important to fabricate a high quality SGOI substrate with low defect density and high Ge content. The higher Ge content in SiGe layer, the smaller lattice mismatch will exist between SiGe and Ge, GaAs or other III–V compounds, which is beneficial for heteroepitaxy.

Tezuka et al. have proposed a Ge condensation technique to fabricate SGOI [8] and the mechanism of the condensation process has been investigated in detail [9]. In the condensation technique a SiGe layer is grown directly on SOI wafer, the Si atoms in SiGe are preferentially oxidized and the Ge atoms from SiGe are condensed into SOI to form a new SGOI structure with higher Ge fraction. Using this method Nakaharai et al. have fabricated a strained GeOI structure with a 7-nm-thick Ge layer [10], but the stacking faults (SF) dislocation formation was not mentioned in this process. Sugiyama et al. also have proposed a two-step oxidation and condensation process (oxidized first at 900 °C and then at 1200 °C) to form SGOI structure with low threading dislocation density [11]. However, the SiGe layer fabricated by this method may not meet the application requirements because of a too low Ge fraction (20%).

In this work, our target is to develop a proper condensation process to fabricate a high Ge content SGOI with low defect density. We have studied the formation and elimination of stacking faults in condensation process. Finally, a modified condensation process is proposed for high quality SGOI fabrication.

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0169-4332/$ – see front matter.
doi:10.1016/j.apsusc.2009.04.162

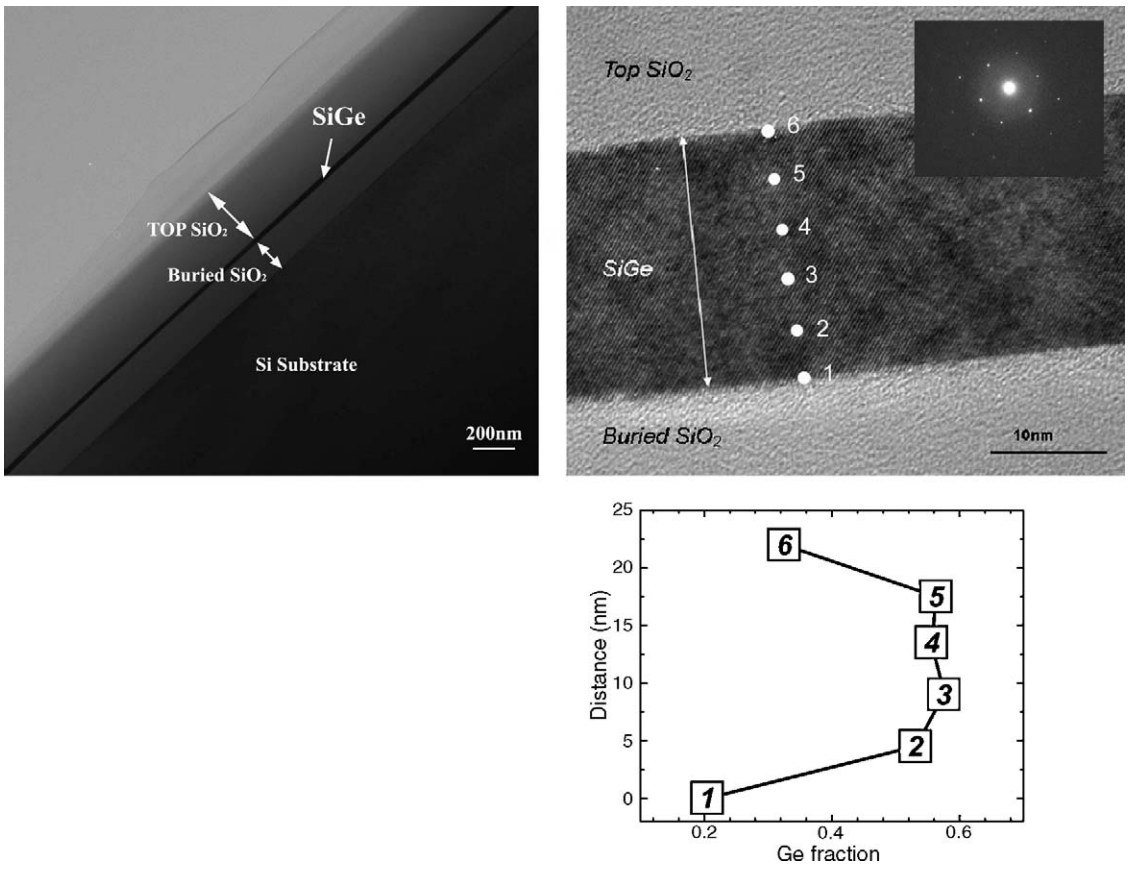

Fig. 1. Cross-sectional TEM images of sample 1 oxidized at 1150 °C for 2.5 h and 900 °C for 1 h. The Ge profiles across the layer as measured by EDS are also shown.

2. Experiment

SGOI substrates were fabricated by oxidation of a sandwiched structure of Si (20 nm)/$Si_{0.85}Ge_{0.15}$ (100 nm)/Si. The SiGe layer (100 nm) and Si cap (20 nm) were grown on the ultrathin SOI substrate (thickness of top Si is 50 nm) by ultra high vacuum chemical vapor deposition (UHVCVD), the process temperature is 500 °C. All the samples were first oxidized for 2–3 h at 1150 °C in dry O_2 and then annealed in N_2 for 1 h at 900 °C. The second oxidation step was carried out at 900 °C for 1 h (sample 1) and 3 h (sample 2). Finally the sample 1 and sample 2 were annealed in N_2 again at 900 °C for more than 3 h to homogenize the Ge fraction in the SiGe layer. Since the oxidation temperature is a key role in the condensation process, the second oxidation or annealing temperature is chosen carefully based on the phase diagrams of Si_xGe_{1-x}. It is not advisable to continue the condensation at a temperature over the melting point of Si_xGe_{1-x}, otherwise it may generate a metastable SiGe layer [4]. The cross-section of SGOI structure is studied by transmission electron microscopy (TEM) and the threading defect density in SiGe layer is evaluated by an enhanced secco etching method [12]. The distribution of Ge atoms in SiGe is obtained by energy dispersive X-ray spectroscopy (EDS) in conjunction with TEM, the spatial resolution is around 1 nm. After removing the top SiO_2 using a diluted HF solution, the SGOI surface roughness is measured using atomic force microscopy (AFM).

3. Results and discussion

3.1. Fabrication of $Si_{0.45}Ge_{0.55}$OI and the formation of stacking faults (SF) dislocations

After the first step oxidation, the thickness and crystal quality of the SiGe layer were characterized by cross-sectional TEM. As shown in Fig. 1, the thickness of SiGe layer in sample 1 is 23 nm. The SiGe layer has preserved its single-crystal lattice structure and shows a smooth SiGe/SiO_2 interface. The single crystal is also confirmed from the electron-beam diffraction inset. The Ge profile obtained by EDS measurements (points 1–6) are also shown in Fig. 1. The Ge fraction of test points 2–5 is around 55% with good uniformity, but lower Ge fraction is observed for test points 1 and 6. The reduction may be induced by the interruption of the SiO_2 near the interface. These data show that most of the Ge atoms are condensed into the remaining SiGe layer during oxidation, but about 15% Ge in the as-deposited sample escapes or is oxidized at the interface. This is because of the competition between Ge diffusion and accumulation at the SiO_2/SiGe interface, excessive oxygen at the interface results in the oxidation of a few Ge atoms accumulated. The SiO_2/SiGe/SiO_2 interfaces in Fig. 1 are sharp and integrated, no undesired amorphous SiGeO is observed at the SiGe/SiO_2 interface.

For sample 1, however, a high density of stacking faults (SF) generated in the SiGe layer is also observed by TEM (shown in Fig. 2). The observed defects here are inclined to {1 1 1} stacking faults. The generation of stacking faults can be explained by a strain relaxation mechanism [5]. During the condensation process, the dislocations are found to form at the initial SiGe/SOI interface and their fragments rise up toward the surface, which is a mechanism for the generation of remaining threading dislocations [13]. Most dislocations in diamond cubic semiconductors are the 60° dislocations (with Burger's vectors $b = a/2\ \langle 1\ 1\ 0\rangle$). Due to the energetic consideration, the 60° dislocations may be dissociated into two partial dislocations of Burger's vectors equal to $a/6\ \langle 2\ 1\ 1\rangle$ and $a/6\ \langle 1\ \bar{1}\ 2\rangle$, which are so called 30° and 90° dislocations [14,15]. These two dislocations repel each other and slip along their common {1 1 1} planes, finally bring the stacking faults (SF) on {1 1 1} planes. In this study, the SF defects in Fig. 2 are present from