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Electrical properties of purified solar grade silicon substrates using a combination of porous silicon and $SiCl_4$

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Abstract

This work investigates the photo-thermal treatment of solar grade (SG) silicon to reduce impurities to a low level suitable for high efficiency low-cost solar cells application. It describes experiment carried out by using a tungsten lamps furnace (rapid thermal processing, RTP) to purify solar grade silicon wafers using a combination of porous silicon (PS) and silicon tetrachloride. This process enables to attract the impurities towards the porous layer where they react with $SiCl_4$ to form metallic chlorides. The gettering effect was studied using the Hall Effect and the Van Der Pauw methods to measure the resistivity, the majority carrier concentration and mobility. We have obtained a significant improvement of the majority carrier mobility after such thermo-chemical treatment. The gettering efficiency is also evaluated by the relative increase of the minority carrier diffusion length *L*, measured by the light beam induced current (LBIC) technique.

Keywords: Silicon; Porous silicon; Silicon tetrachloride; Gettering

1. Introduction

Photovoltaic industry can accept low purity silicon (solar grade silicon "SGS") compared to semiconductor industry. Purity requirements and potential production techniques for solar grade silicon have been widely studied [1–3]. For solid phase purification or impurities gettering in silicon, several techniques were used to reduce impurity concentrations in the device region of the wafer by localizing them in separate predefined regions of the wafer where they cannot affect the device performances. The most interesting techniques are internal gettering that uses silicon oxide precipitates as gettering sites [4–6], segregation gettering in p/p^+ structures which is driven by the enhanced solubility of metals in the heavily doped substrate [7–9], gettering by ion implantation is another proximity gettering technique [10,11]; the atoms used for implantation are usually light elements (such as hydrogen, helium, boron, carbon, oxygen, etc...), in order to avoid amorphization of the near-surface region. Gettering of impurities by the formation of a thin porous silicon (PS) layer followed by a thermal annealing in a nitrogen or oxygen atmosphere has been recently used [12,13]. In this paper, we present the possibility of gettering impurities from solar grade silicon by photo-thermal annealing (PTA) in $SiCl_4/N_2$ atmosphere using a thin porous silicon layer on both sides of the wafer. The gettering effect was studied using the Hall Effect and the Van Der Pauw methods, and light beam induced current (LBIC) measurements.

2. Experimental procedures

The substrates used are Czochralski (Cz) solar grade (1 0 0) oriented, p-type boron doped silicon wafers, with a resistivity ranging from 1 to 3 Ω cm and a thickness of 450 μm. The wafers were dipped in an acid mixture solution (HF: 16%, HNO_3: 64%, CH_3COOH: 20%) for a few seconds in order to obtain a cleaned surface, required for homogeneous porous layer formation, then rinsed in deionezed water. A thin porous layer was formed on both sides of the sample by stain-etching the silicon wafers in a ($HF/HNO_3/H_2O$) solution with (1:3:5) volume composition. The

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next step consists to heat samples in a tungsten lamps furnace under $SiCl_4/N_2$ atmosphere at various temperatures (from 850 to 1000 °C) for various annealing durations (from 30 to 90 min). The samples are placed in a closed quartz reactor. Then the reactor is purged with nitrogen in order to remove oxygen and other gases, which can be a contamination sources for the samples. After 15 min of purge the sample is heated from ambient to the annealing temperature under nitrogen atmosphere. After reaching the annealing temperature a $SiCl_4$ gas flow (obtained by bubbling nitrogen through $SiCl_4$) is established in the reactor during a period that differs from a sample to another. Finally, the sample is cooled in a nitrogen atmosphere. After removing the samples from the reactor, they were successively immersed in a diluted HF then in a NaOH (1N) solution, in order to remove eventual silicon oxides and the PS layers, respectively. The wafers to be studied were separated in two sets. The first set will be used for resistivity and Hall Effect measurements. The second set will be used to develop an metal insulator semiconductor (MIS) structure, whose realisation is described elsewhere [13]. The MIS structure is exploited to characterise the device by the light beam induced current technique.

3. Results and discussions

After removing the porous silicon layer the resistivity was measured using the Van Der Pauw method. Fig. 1 shows two resistivity profiles corresponding to an untreated sample (used as a reference) and a sample photo-thermal annealed in a tungsten lamps furnace at 950 °C under a $SiCl_4/N_2$ atmosphere during 60 min. One can notice that the latter PTA conditions reduce the resistivity on a depth of about 45 μm on both sample sides. At a first sight this resistivity reduction could be due to impurities migration, during the process, from the bulk towards the porous silicon layer as has been shown elsewhere [13]. The $SiCl_4$ related chlorine is known to react with metallic impurities (Al, Ca and Mg) [2]. In fact, at high temperatures metallic impurities decomposes the $SiCl_4$ to form silicon and metallic chlorides. All metallic chlorides are produced in gas form, and thus are easily extracted. Furthermore, the deposit presents many dangling

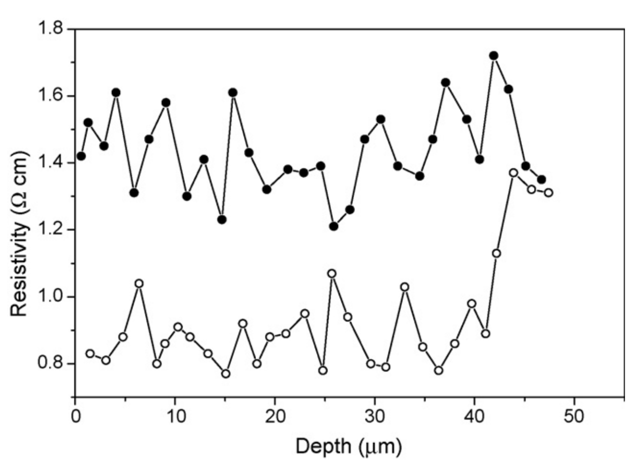

Fig. 1. Variation of the resistivity with depth for an untreated sample (filled circles) and an annealed sample at 950 °C for 60 min in $SiCl_4/N_2$ atmosphere (open circles).

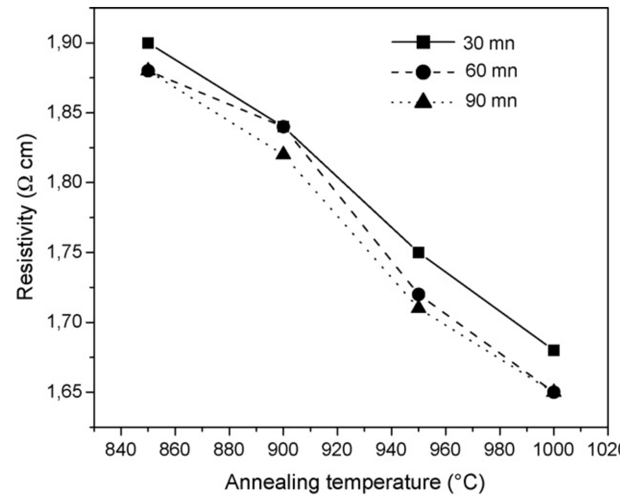

Fig. 2. Variation of the resistivity as a function of annealing temperature for various annealing durations under a $SiCl_4/N_2$ atmosphere.

bonds that may attract further impurities towards the surface. Fig. 2 illustrates the variation of the resistivity of the silicon wafers with annealing temperature for various heat treatment durations. One may notice that the resistivity decreases when increasing the annealing temperature.

This resistivity lowering is probably due to bulk defects reduction. In Table 1, we report the evolution of the carrier mobility with treatment conditions. Treatment at 1000 °C and N_2 ambient without PS does not have any significant effect on the mobility of the majority carrier (132 $cm^2 V^{-1} s^{-1}$) as compared to the reference sample (97.7 $cm^2 V^{-1} s^{-1}$). Treatment under the preceding conditions in presence of a PS layer leads to an enhancement of the mobility (i.e., 709 $cm^2 V^{-1} s^{-1}$) about seven times more than that of the reference sample. This result shows the importance of porous silicon layer in the gettering process. When the same treatment is done in $SiCl_4/N_2$ ambient in presence of a PS layer the mobility reaches a value of 1417 $cm^2 V^{-1} s^{-1}$ (cf. Table 1). The presence of $SiCl_4$ leads to a mobility, which is two orders of magnitude greater than that in pure N_2 ambient. This spectacular enhancement of the mobility is probably due to the reaction of the $SiCl_4$ with impurities trapped within the porous layer and attraction of additional impurities after the gaseous reaction products were extracted.

Now, we will essentially focus our study on silicon wafers photo-thermally annealed under $SiCl_4/N_2$ atmosphere. Fig. 3

Table 1
Effect of treatment conditions on the majority carrier mobility in silicon substrates

Sample number	Treatment conditions	Mobility ($cm^2 V^{-1} s^{-1}$)
1	Untreated sample (reference)	97.7
2	Sample without a porous layer treated at 1000 °C in N_2 atmosphere	132
3	Sample with a porous layer treated at 1000 °C in N_2 atmosphere for 90 min	709
4	Sample with a porous layer treated at 1000 °C in $SiCl_4/N_2$ atmosphere for 90 min	1417