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Fabrication of combinatorial nm-planar electrode array for high throughput evaluation of organic semiconductors

M. Haemori [a,*], T. Edura [b], K. Tsutsui [b], K. Itaka [a,c], Y. Wada [b,c], H. Koinuma [a,c,d]

[a] *Materials and Structures Laboratory, Tokyo Institute of Technology, 4259 Nagatsuta, Midori-ku, Yokohama 226-8503, Japan*
[b] *Nanotechnology Research Laboratory, Waseda University 513 Wasedatsurumaki, Shinjuku-ku, Tokyo 162-0041, Japan*
[c] *CREST-JST, 4-1-8 Honcho, Kawaguchi, Saitama 332-0012, Japan*
[d] *NIMS-COMET, 1-2-1 Sengen, Tsukuba, Ibaraki 305-0047, Japan*

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Abstract

We have fabricated a combinatorial nm-planar electrode array by using photolithography and chemical mechanical polishing processes for high throughput electrical evaluation of organic devices. Sub-nm precision was achieved with respect to the average level difference between each pair of electrodes and a dielectric layer. The insulating property between the electrodes is high enough to measure *I–V* characteristics of organic semiconductors. Bottom-contact field-effect-transistors (FETs) of pentacene were fabricated on this electrode array by use of molecular beam epitaxy. It was demonstrated that the array could be used as a pre-patterned device substrate for high throughput screening of the electrical properties of organic semiconductors.

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Keywords: Combinatorial electrodes; Nm-planar; Organic semiconductor; Chemical mechanical polishing; High throughput

1. Introduction

Organic field-effect-transistors (FETs) have attracted tremendous attention, due to their potential application in low-cost large-area flexible displays and electronics [1,2]. The variety of derivatives of organic materials provides a promising potential for new functional materials. New organic materials with the possibility of device application are being synthesized by chemists on a day-to-day basis. Because electric devices are composed of several different layers such as electrode and dielectric layers, the optimization of these

* Corresponding author. Fax: +81 45 924 5377.
E-mail address: koinuma1@oxide.msl.titech.ac.jp (M. Haemori).

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layers and their dimensions requires much time and intense effort. Thus, it is difficult to find serendipitous candidates for organic semiconductors from the enormous number of possible organic materials.

These issues can be very efficiently and elegantly handled by the combinatorial method. The concept of the combinatorial method consists of two factors: large-scale paralleled synthesis and high throughput screening [3]. The integrated circuit (IC) process, including microelectro-mechanical systems (MEMS), is a powerful method with which to realize the large-scale synthesis of devices. Recently, combinatorial substrates with mechanical cantilevers were used for investigating ferroelectrics oxides [4]. However, very few results have been reported on the application of the combinatorial method for investigating the electrical properties of organic semiconductors [5].

In this paper, we report a novel approach to screen the electrical properties of organic semiconductors. We successfully fabricated integrated electrodes on a Si/SiO_2 substrate by using photolithography and chemical mechanical polishing (CMP) processes. This combinatorial electrode array chip, which has two remarkable advantages over conventional structures, viz., the electrodes were combinatorially designed to have various combinations of channel widths ($W = 10$–$100\ \mu m$) and channel lengths ($L = 0.7$–$20\ \mu m$) of FETs, and the other is that they have a flattened structure between the electrodes and the dielectric layer interface (i.e., the electrodes are embedded in the insulating layer). This flatness enables us to observe the organic nanostructure within the electrode gap after deposition and confirm structural effects on the grains. This pre-patterned device substrate is useful for the simultaneous high throughput investigation of the electrical properties of organic semiconductors and their structural contributions.

2. Experimental

Fig. 1 shows a schematic diagram of the processing steps for fabricating the combinatorial nm-planar electrode array. The substrate was heavily doped n-type Si with a 500-nm thick layer of thermally grown silicon dioxide (SiO_2). Initial cleaning of the substrate was done by soaking in hot H_2SO_4:H_2O_2 (1:1) solution for 10 min, then rinsing thoroughly with deionized water (Fig. 1(a)).

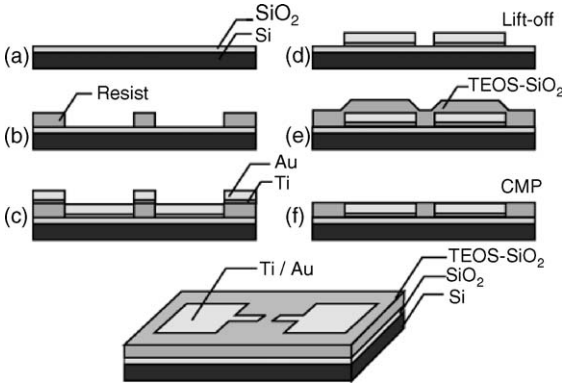

Fig. 1. Schematic diagram of the processing steps for fabricating our combinatorial nm-planar electrode array: (a) the substrate was thermally grown SiO_2 on Si; (b) electrodes patterning by use of photolithography; (c) Ti and Au as electrodes (source and drain contacts) material were deposited by electron beam deposition; (d) development and lift-off; (e) TEOS-SiO_2 deposited onto substrate entirely; (f) dielectric layer polished by CMP.

The lithography process steps for fabricating the electrode pattern are shown in Fig. 1(b). First, hexamethyldisilazane (HMDS) was coated with a spin-coater (4000 rpm, 10 s) to modify the SiO_2 surface. Then, positive photo-resist (TSMR-V90-15cp) was coated on the substrate (700 rpm, 5 s and 2000 rpm, 30 s) and baked on a hotplate (100 °C, 60 s). The resist layer was exposed by use of a chrome mask with various electrode patterns followed by a post-exposure baking (110 °C, 90 s). It was then submerged in developer to produce a positive image of the electrode pattern (60 s). Thus, the objective electrode patterns were delineated by immersing the substrate.

The substrate thus prepared was deposited with a 20-nm thick Ti layer and an 80-nm thick Au layer successively by electron beam deposition to form the electrodes (source and drain contacts) (Fig. 1(c)). The substrate was soaked in acetone and methanol to lift-off the metal layers and to form the electrode structures and was subsequently rinsed with deionized water (Fig. 1(d)).

Then, a 300-nm thick SiO_2 layer was deposited by the plasma chemical vapor deposition (CVD) method with tetraethoxysilane (TEOS) as a source material; the substrate temperature was 300 °C. The TEOS-SiO_2 layer was used as a gate insulator of the FET, as indicated in Fig. 1(e).