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Electrical and structural properties of a stacked metal layer contact to *n*-InP

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ABSTRACT

In this study, we found that the double metal contact structure in Pt/Al/*n*-InP diodes provides better rectification characteristics than conventional single-metal/*n*-InP Schottky diodes. The effective barrier height was measured to be 0.67 eV for a 400 °C-annealed Pt/Al/*n*-InP diode sample. The increase in the barrier height is attributed to the formation of Al_2O_3 at the metal/*n*-InP contact interface during thermal annealing. The formation of the phase Al_2O_3 phase was monitored by X-ray diffraction (XRD) analysis. The corresponding element profiles of Al and O were also confirmed at the metal/*n*-InP contact interface using secondary ion mass spectrum (SIMS) analysis. The lowering of the Schottky barrier height due to the inhomogeneity at the metal/*n*-InP junction is also discussed on the basis of the TE theory. The distribution of local effective Schottky barrier heights was explained by a model incorporating the existence of double Gaussian barrier heights, which represent the high barrier and low barrier of the full distribution in the temperature ranges of 83–198 and 198–300 K.

1. Introduction

InP exhibits high electron mobility, a large and direct band gap, high saturation velocity, and a large breakdown voltage. These qualities make it a promising semiconductor for use in high-speed metal–semiconductor field-effect transistors (MESFETs) [1–3], electro-optical devices [4], and laser diodes [5].

However, surface Fermi level pinning, which occurs due to the high density of surface states and other nonstoichiometric defects, makes it difficult to obtain a Schottky barrier height greater than 0.5 eV in *n*-InP [6–8]. This low barrier height is responsible for the large reverse leakage current and the consequent poor electrical performance in *n*-InP-based Schottky diodes. Therefore, achieving a high Schottky barrier height is an important research issue in InP device development. Forming an insulating layer between metal and InP—which makes it a metal–insulator–semiconductor (MIS) diode—improves the electrical characteristics of InP contacts. Techniques to achieve this for *n*-InP include PH_3 plasma treatments [9]; growing a thin P_3N_5 [10] or $PO_xN_yH_z$ [11] or InSb [12] film or an interfacial oxide layer [13–16]; low-temperature deposition techniques [17]; or using stacked metal structures such as Ag/Al [18], Pt/Al [19], and Ni/Ai/Ni [20]. And for *p*-InP contacts, a N_2O layer [21] deposited between the metal and the semiconductor was shown to improve the diode's electrical characteristics. All of the above studies have reported greater effective barrier height than that of a conventional single metal/*n*-InP diode.

In this paper, we discuss the electrical characteristics of a Pt/Al/*n*-InP diode that have been determined using temperature dependent current–voltage (*I–V–T*) measurements. First, we discuss the transformation of the microstructures of the diode after thermal annealing, monitored by X-ray diffraction (XRD) and secondary ion mass spectrum (SIMS) analyses. Second, we discuss the temperature dependence of barrier height and ideality factor on the basis of TE theory in which the barrier heights have a Gaussian distribution around a mean value due to barrier height inhomogeneities at the metal–semiconductor interface. These effects are discussed with respect to the *I–V–T* measurements for the diodes that were taken at temperatures in the range of 83–300 K.

2. Experimental

Undoped, native *n*-type InP(1 0 0) with carrier concentration of approximately $-9 \times 10^{15}\,cm^{-3}$ was used as the substrate for the Schottky diode. A backside Ohmic contact with a low specific contact resistance was formed at the beginning of the process by evaporating a AuGeNi eutectic source (84% Au, 12% Ge, and 4% Ni by weight), followed by annealing at 400 °C for 3 min. An InP wafer was capped on the front surface of the substrate to prevent out-diffusion of phosphorus during the annealing process. The wafers were then degreased with trichloroethylene (TCE), acetone (ACE), methanol, and de-ionized water, in that order, and cleaned by soaking them in H_2SO_4 (98%) for 3 min. They were then etched in a $NH_4OH:H_2O_2:H_2O = 3:1:15$ solution for 3 min to remove surface damage. A 2000-Å-thick layer of SiO_2 was then deposited on

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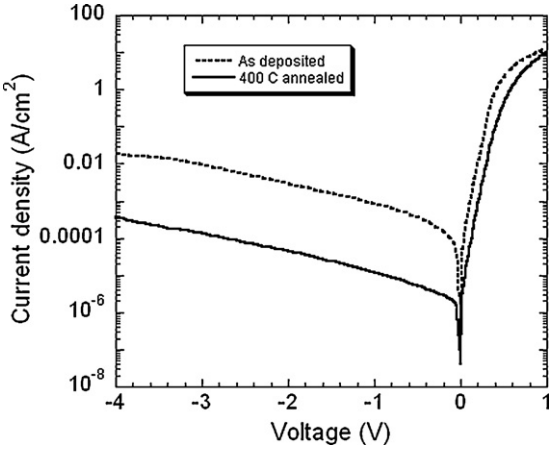

Fig. 1. The *I–V* characteristics of the Pt/Al/*n*-InP diode with 400 °C-annealing and without annealing.

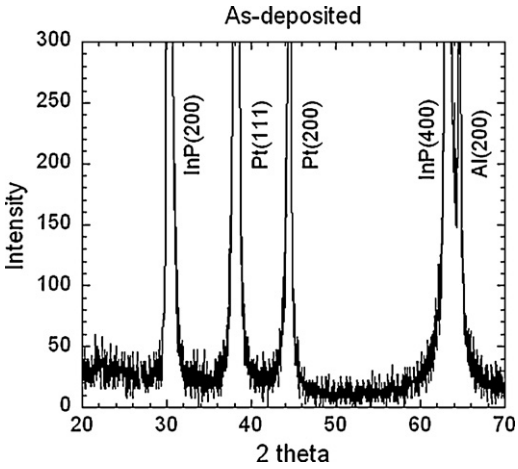

Fig. 2. The XRD spectrum of the unannealed Pt/Al/*n*-InP diode.

the front of the wafers for isolation purposes, and the contact patterns were defined photo-lithographically. The SiO_2 in the contact windows was etched in buffered oxide etch (BOE), and then the wafers were rinsed in de-ionized water. An 85-Å-thick layer of Al was deposited on the wafers and on this layer a 500-Å-thick layer of Pt was subsequently deposited, in a vacuum of 4×10^{-6} Torr. The metal patterns were defined using a lift-off process. The surface area of the diode was 4.6×10^{-4} cm^2. The samples were then annealed in an N_2 gas flow, at a varying temperature for a long time. The *I–V* characteristics were measured with a semiconductor parameter analyzer. To evaluate the distribution of elements in the deposited films, SIMS analysis was performed with a primary beam of 133Cs$^+$ at 10 keV, at a current of 16 nA and over rastering area of 225 μm × 225 μm. XRD analysis was employed to observe the phase formation in the samples after variable temperature annealing.

3. Results and discussions

The effective barrier height ϕ_b and ideality factor n were determined by using the TE current voltage expression [6]:

$$I = I_s \left[\exp\left(\frac{q(V - IR_s)}{nkT} \right) - 1 \right] \quad (1)$$

where

$$I_s = AA^*T^2 \exp\left[\frac{-q\phi_b}{kT} \right] \quad (2)$$

R_s is the series resistance of the diode, V is the applied voltage, q is the electronic charge, k is the Boltzmann constant, T is the absolute temperature, A is the area of diode, A^* is the effective Richardson constant, ϕ_b is the effective Schottky barrier height at zero bias, and n is the ideality factor. The theoretical A^* value of 9.4 A cm^{-2} K^{-2} is used for InP. The saturation current density J_s was obtained by extrapolating the linear region of the forward-bias semi-log *I–V* curves to the zero applied voltage and the ϕ_b values were calculated from Eq. (2). The values of n were determined from the slope of the linear region of the forward bias semi-log *I–V* characteristics using the relation: $n = q/kT[\partial V/\partial(\ln J)]$. Note that n depends on the current flow at the interface and is equal to 1 for an ideal diode.

Fig. 1 shows the *I–V* characteristics of the Pt(500 Å)/Al(85 Å)/*n*-InP Schottky diode with and without annealing. The measurements revealed an increase in the barrier height after annealing. The barrier height and the ideality factor before annealing were 0.64 eV and 1.35, respectively. In contrast, the barrier height and the ideality factor for the 400 °C-annealed diode were 0.67 eV and 1.17, respectively. The reverse leakage of the annealed diode was drastically lower than that of the unannealed diode. This was due to the rectification effect of the Al_2O_3 at the junction interface. There was also an improvement in the ideality factor after annealing. Owing to the annealing at 400 °C for 10 min, the interface states between metals and InP substrate were reduced, which resulted in a decrease in the generation and recombination effects at the junction.

The phase changes in the thin metal film and the reaction between metal and substrate during thermal annealing were monitored by XRD analysis. The XRD analysis for the unannealed Pt/Al/*n*-InP diodes (Fig. 2) contains signal peaks centred at diffraction angles 2θ 30.3° and 63.2°, which indicate InP(2 0 0) and InP(4 0 0), respectively. The signal peaks for Pt are centred at $2\theta = 38.5°$ and $2\theta = 44.3°$, which indicate Pt(1 1 1) and Pt(2 0 0), respectively. The Al signal is found at $2\theta = 64.4°$, which corresponds to Al(2 0 0).

Fig. 3 shows the spectrum of the diode after it was furnace annealed at 400 °C. The diffraction spectrum is similar to that of the unannealed sample except for the strong signal corresponding to the newly grown phase that is centred at $2\theta = 21.4°$, which is indexed to Al_2O_3(1 1 2) [22]. Compared with the XRD patterns for the unannealed samples, the Al_2O_3(1 1 2) peak in the spectra of the 400 °C-annealed sample had a strong intensity. This means there was a better crystallization of the Al_2O_3(1 1 2) phase after the 400 °C annealing. The spectrum also shows that the intensity of the InP signal is weaker for the unannealed sample as compared to that of the 400 °C annealed sample. Because the out-diffusion of

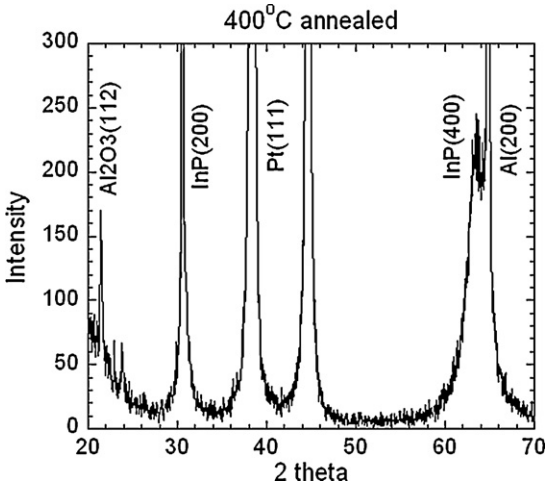

Fig. 3. The XRD spectrum of the 400 °C-annealed Pt/Al/*n*-InP diode.