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# Surface passivation of III–V semiconductors for future CMOS devices—Past research, present status and key issues for future

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ABSTRACT

Currently, III–V metal–insulator–semiconductor field effect transistors (MISFETs) are considered to be promising device candidates for the so-called "More Moore Approach" to continue scaling CMOS transistors on the silicon platform. Strong interest also exists in III–V nanowire MISFETs as a possible candidate for a "Beyond CMOS"-type device. III–V sensors using insulator–semiconductor interfaces are good candidates for "More Moore"-type of devices on the Si platform. The success of these new approaches for future electronics depends on the availability of a surface passivation technology which can realize pinning-free, high-quality interfaces between insulator and III–V semiconductors.

This paper reviews the past history, present status and key issues of the research on the surface passivation technology for III–V semiconductors. First, a brief survey of previous research on surface passivation and MISFETs is made, and Fermi level pinning at insulator–semiconductor interface is discussed. Then, a brief review is made on recent approaches of interface control for high-k III–V MIS structures. Subsequently, as an actual example of interface control, latest results on the authors' surface passivation approach using a silicon interface control layer (Si ICL) are discussed. Finally, a photoluminescence (PL) method to characterize the interface quality is presented as an efficient contactless and non-destructive method which can be applied at each step of interface formation process without fabrication of MIS capacitors and MISFETs.

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## 1. Introduction

According to major silicon electronics industries including Intel Corp. [1,2], the ultimate scaling limit of the Si CMOS (complementary metal-oxide–semiconductor) technology is rapidly approaching, as evidenced on the famous International Technology Roadmap for Semiconductors (ITRS) [3]. Because of this, intensive research on III–V MISFETs has come back after many years as a part of efforts to search for suitable device candidates which fit in the so-called "More Moore Approach" to continue scaling CMOS transistors on the silicon platform. Furthermore, strong interest also exists in III–V nanowire MISFETs as a possible candidate for a "Beyond CMOS"-type device, as favourably evaluated on the emerging research device (ERD) division of the ITRS [4]. Additionally, III–V sensors using insulator–semiconductor interface are good candidates for "More Moore"-type of devices on the Si platform. The success of above new approaches for future electronics depends on the availability of a surface passivation technology which can realize pinning-free, high-quality interfaces between insulator and III–V semiconductors.

The purpose of the present paper is to review the past history, present status and key issues of research on surface passivation technologies for III–V semiconductors aiming at "More Moore", "More than Moore" and "Beyond CMOS" devices. The paper covers the following topics. In the first place, a brief survey of previous research on surface passivation and III–V MISFETs is made, and the Fermi level pinning phenomena at the insulator–semiconductor interface of III–V materials are discussed. Then, a brief review is given on more recent approaches for interface control for high-k III–V MIS structures. Subsequently, detailed latest results on the authors' approach using a silicon interface control layer (Si ICL) are presented and discussed. Finally, a photoluminescence (PL) method to characterize the interface quality is presented. It is an efficient contactless and non-destructive method which can be applied at each step of interface formation process without fabrication of MIS capacitors and MISFETs.

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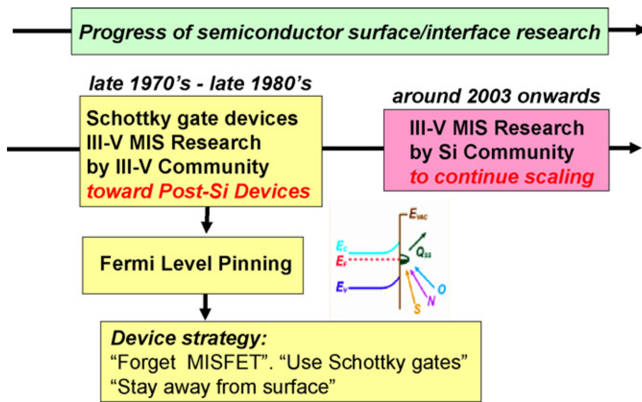


**Fig. 1.** History of III–V FET device development.

## 2. Fermi level pinning at III–V interfaces

### 2.1. Brief survey of III–V FET device research

Field effect transistors (FETs) are key devices in III–V electronics as well as in Si electronics. The evolution of III–V FET research is briefly summarized in Fig. 1. The first III–V FET operating in the microwave region was the GaAs metal–semiconductor FET [5,6], usually abbreviated as MESFET. This device uses a Schottky gate for control of the carrier flow. Then, as a natural extension from the Si MOSFET, intensive research efforts were started in the III–V community from late 1970s up to late 1980s to develop high-performance metal–insulator–semiconductor (MIS) FETs on III–V materials such as GaAs, InP and related compounds. However, these efforts were not successful due to the Fermi level pinning at insulator–semiconductor interface whose details are discussed later. Fortunately, the high electron mobility transistor (HEMT) using the AlGaAs/GaAs heterointerface [7] was invented out of such efforts, and opened up a new era of the heterostructure electronics, including MESFETs, HEMTs, heterojunction bipolar transistors (HBTs), solar cells, light emitting diodes, lasers, etc.

On the other hand, the above-mentioned Fermi level pinning phenomenon at the insulator–semiconductor interface could only produce MISFETs with very poor control of carrier flow and various instabilities such as hysteresis and drain current drift. Particularly, realization of n-channel enhancement mode GaAs MISFETs by surface inversion was extremely difficult, and most of the GaAs MISFETs were depletion mode devices. It was also found that the Fermi level pinning takes place also at air-exposed surfaces of the III–V semiconductors, resulting in formation of a surface depletion layer in GaAs and related compounds. Because of these, the strategies for III–V device development became "forget about MISFETs", "use Schottky gates" and "stay away from surface".

Typical structures of practical III–V FETs are shown in Fig. 2(a)–(c). They all utilize Schottky gates. As for the surface of the device, the recessed gate MESFET shown in Fig. 2(a) tries to make the free surface to lie as far as possible from the channel region to minimize the effect of surface depletion on the access resistance. The self-aligned MESFET with a refractory metal gate [8], shown in Fig. 2(b), avoids the low-doped access region of the channel by using a self-aligned gate. Another well-known self-aligned structure is the SAINT (self-aligned implantation for n+-layer technology) device [9] using a non-refractory gate, which also avoids the low-doped access channel region by self-alignment. The HEMT shown in Fig. 2(c) can be regarded as an MISFET with a widegap AlGaAs layer acting as a gate insulator. However, unlike the usual insulator–GaAs interface, the AlGaAs/GaAs heterointerface is free from Fermi level pinning and realizes almost ideal gate control. Furthermore, the top $n^+$ cap layer minimizes the effect of surface depletion due to Fermi level pinning at the surface.

These devices were developed at that time as candidates aiming at "post-Si" devices which unfortunately never became reality in the last century due to continued progress of the silicon devices. However, these devices as well as their advanced versions [10] using high-mobility channel materials such as lattice matched or pseudomorphic InGaAs on the InP substrate, or metamorphic InGaAs on the GaAs substrate, are now widely utilized as key devices in the optical and wireless communication. Nitride based FETs such as AlGaN/GaN HEMTs which appeared in 1990s are now opening up new areas in high-frequency high-power applications [11]. Thus, the progress of III–V communication devices will continue as indicated on the ITRS for rf devices [12]. Furthermore, use of nitride devices for low-frequency power electronics is attracting attention. Thus, usefulness of III–V devices has been industrially established in spite of the fact that the Fermi level pinning issue has not been satisfactorily solved.

In addition to the above situation of III–V FETs, strong interests have recently now come back to III–V MISFETs, rather suddenly after so many years as shown in Fig. 1. This new trend is not for the communication application, but for the high-speed logic application where they are used on the Si platform to continue scaling of CMOS transistors, as explained in Section 1. The new trend started

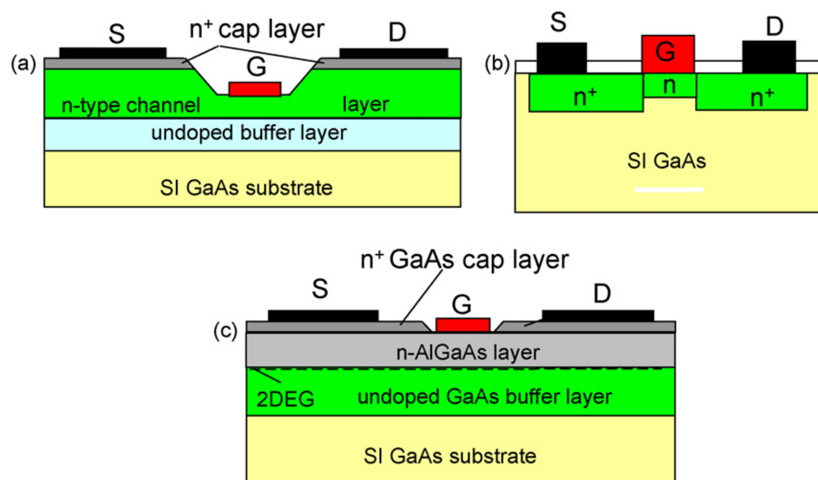


**Fig. 2.** Typical structures of practical III–V FET devices. (a) Recessed gate MESFET, (b) self-aligned gate MESFET, and (c) HEMT.

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